Electrical performance analysis of double gate transistor (DGMOS)

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Abstract— **We present in this paper the main results of a two-dimensional numerical study based on the finite difference method. The static current-voltage characteristics I(V) of a double gate MOS transistor (DGMOS) are compared with a single gate MOSFET with SOI (Silicon On Insulate) technology. For this, we use a self consistent calculation of Schrodinger-Poisson coupled equations with pseudo - 2D scheme. Simulation results show that the drain current values of the transistor DGMOS are higher compared with those of the SOI MOS transistor. In addition, the DIBL effect and the leakage current are minimized in the case of DGMOS. This confirms the performances of the double gate transistor and its ability to better control the channel and thus the drain current.**

Keywords- single gate transistorMOSFET, double gate transistor DGMOS, Poisson equation, Schrödinger equation, DIBL, self consistent, leakage current.

I.   INTRODUCTION

The semiconductor industry is always looking for developing semiconductor technology to finer geometries [1, 2].

The aim of the decrease in size of microelectronic devices is to reduce the cost and to improve the performance devices, but this, however, leads to the occurrence of adverse effects. To minimize these latters, it is interesting to turn to new transistor architectures such as double gate MOSFET which is now proving to be a very promising alternative [3, 4, 5].

II.   STRUCTURE STUDIED

The schematic description of double-gate MOS device is shown in Fig.1. It has 10 nm gate length L_G, the gate oxide T_{ox} and Silicon body thicknesses T_{Si} are equal to 1.5 nm. The source and drain lengths L_{SD} are equal to 5 nm. The doping density is $N_D = 10^{20} cm^{-3}$ in N+ source/drain regions and $N_A = 10^{15} cm^{-3}$ in the channel (P type). The work function of the gate material considered is 4.46 eV to achieve the theoretical threshold voltage V_T to 0.2V.
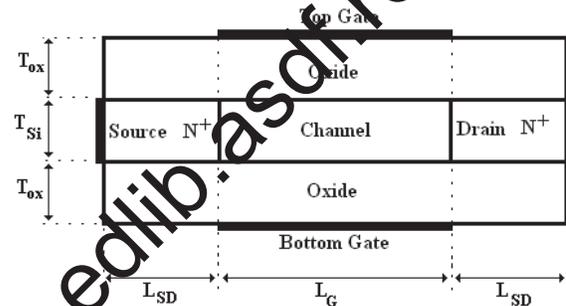

Figure1.   Schematic of double gate structure

We consider, in order to compare the electrical performances, a same transistor as the DGMOS structure (same size, same features) but a single gate one (Fig. 2).
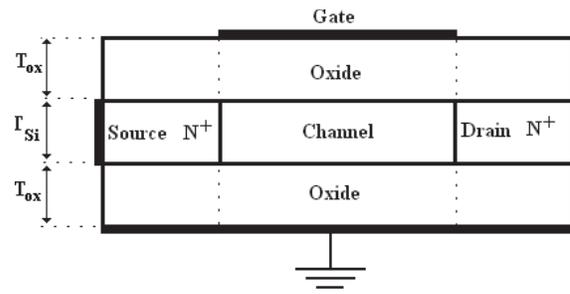

Figure2.   Schematic of single gate structure with SOI technology

III.   FUNDAMENTAL EQUATIONS

The size reduction devices to nanometric sizes reveal quantum phenomena, previously considered largely non-existent or negligible. For this, it is necessary to use equations derived from quantum mechanics [6]. The most rigorous approach is to solve the Poisson and Schrödinger equations simultaneously to take into account the quantum phenomena.

$$\frac{d^2V(x,y)}{dx^2}+\frac{d^2V(x,y)}{dy^2}=-\frac{\rho(x,y)}{\varepsilon_0\varepsilon_r} \quad (1)$$

$$-\frac{h^2}{2m^*}\frac{d^2\psi(y)}{dy^2}+qV(y)\psi(y)=E\psi(y) \quad (2)$$

Where: ψ(y) is the wave function corresponding to the eigenvalue E; V(y): the electrostatic potential and ρ(x) is the charge density.

We clearly see that the equations (1) and (2) are coupled. It is therefore self consistency in their resolution [7, 8, 9]. We can illustrate the self consistent system by the following one:

$$\begin{cases} \rho(y)=S[V(y)] \\ V(y)=P[\rho(y)] \end{cases}$$

Where: the functions S [V(y)] and P [ρ(y)] represent the Schrödinger and Poisson equations.

IV. VALIDATION MODEL

In order to validate the obtained results, we compare our model with Sentaurus numerical simulation (ISE-TCAD software).

The comparison between the modelled and simulated characteristics gives good agreement for V_{GS} down to 0.4 V these devices are operated at V_{GS} lower than 0.4 V (linear regime), and therefore, the model is valid for the regimes of practical interest.
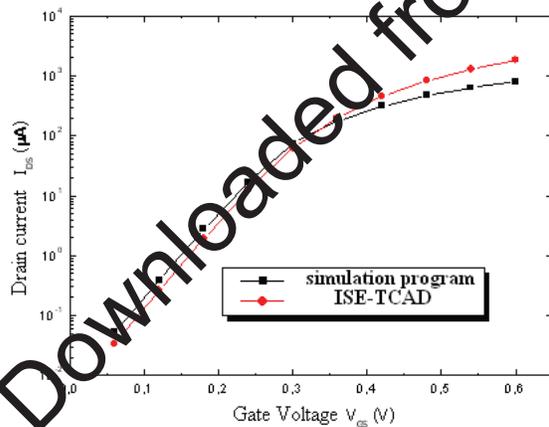
Figure 11. Comparison of the output characteristics between simulation program and ISE-TCAD

V. RESULTS AND DISCUSSIONS

We have considered this model in order to develop our Matlab code [9]. This modelisation was used to compare the both devices. Indeed, Figures 3 and 4 represent the current voltage characteristics I_D (V_{DS}) for single and double gate architectures simulated with L_G = 10 nm respectively for T_{Si} = 2 nm and 1.5 nm.

We observe an increase in the slope of the transistors (single gate and double gate) in the linear regime when the thickness T_{Si} is reduced from 2 to 1.5 nm.
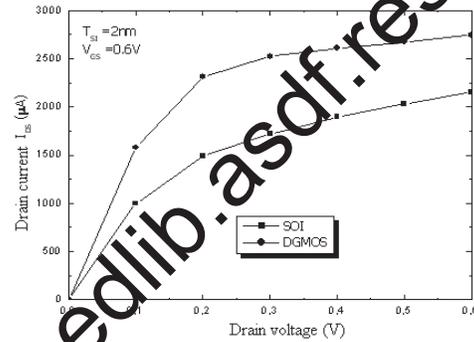
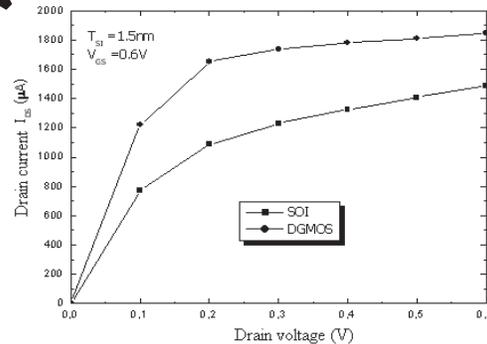Figure 3. I_D vs.V_{DS} for a gate voltage of 0.6V and thickness silicon of 2nm

Figure 4. I_D vs.V_{DS} for a gate voltage of 0.6V and thickness silicon of 1.5 nm

The On-current I_{ON} (saturation current) is more important in the DGMOS compared with single gate transistor. Worth 2150 µA is for SOI MOS transistor and 2745 µA for DGMOS in the case of thickness silicon T_{Si}=2nm.

On the transfer characteristic I_D (V_{GS}) (fig. 5 and 6) we confirm the previous result [I_{ON} (DGMOS)>I_{ON} (SOI)].
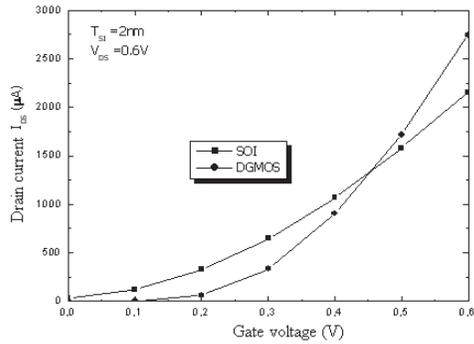
Figure5. I_D vs.V_{GS} for a drain voltage of 0.6V and thickness silicon of 2 nm
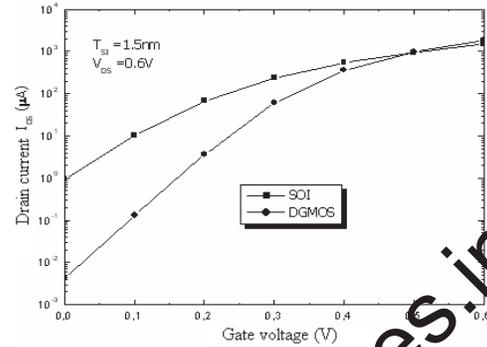

Figure 8. I_D (V_{GS}) characteristics at V_{DS}=0.6V and T_{Si} =1.5 nm

The Off-current (I_{OFF}) is significantly lower in the DGMOS than in the single gate. We can have a better control of the output current by considering DGMOS.

Fig. 9 shows the evolution of the conduction band in the DGMOS device (V_{GS}=0V) for different drain voltage V_{DS}=10mv, 0.2 V and 0.6V with L_G=10nm and T_{Si}=1.5nm. Is clearly shown the Drain Induced Barrier Lowering (DIBL).
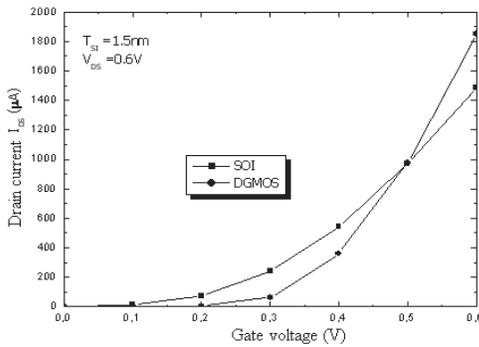

Figure 6. I_D vs.V_{GS} for a drain voltage of 0.6V and thickness silicon of 1.5 nm

The figures 7 and 8 show the characteristics I_D (V_{GS}), in a semi-logarithmic scale, simulated with L_G = 10 nm respectively for T_{Si} = 2 nm and 1.5 nm.
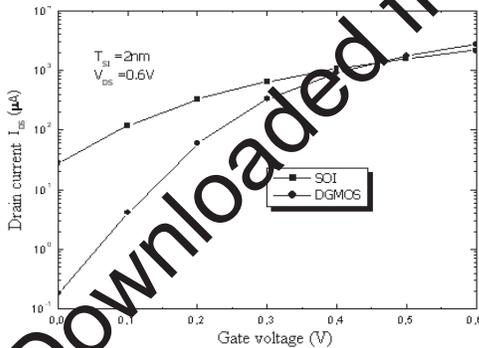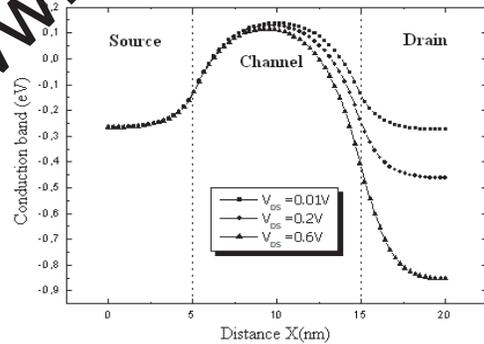

Figure 9.   Conduction Band for differences drain voltage

Fig 10.a and 10.b clearly illustrate that the DIBL effect is lower in DGMOS architecture.

Figure 7. I_D (V_{GS}) characteristics at V_{DS}=0.6V and T_{Si} =2 nm

VI. CONCLUSION

We have present in this paper a self-consistent Poisson and Schrödinger simulation. This method has allowed us to have significant results with good convergence.

We have shown that for a small thickness of the active layer, a best performance is obtained with double gate transistor. More, the analysis of DIBL effect in both single and double gate transistors, confirms that the performances of double gate transistor are better.

Finally, the comparison between our model and Sentaurus numerical simulation gives good agreement for V_{GS} down to 0.4 V.

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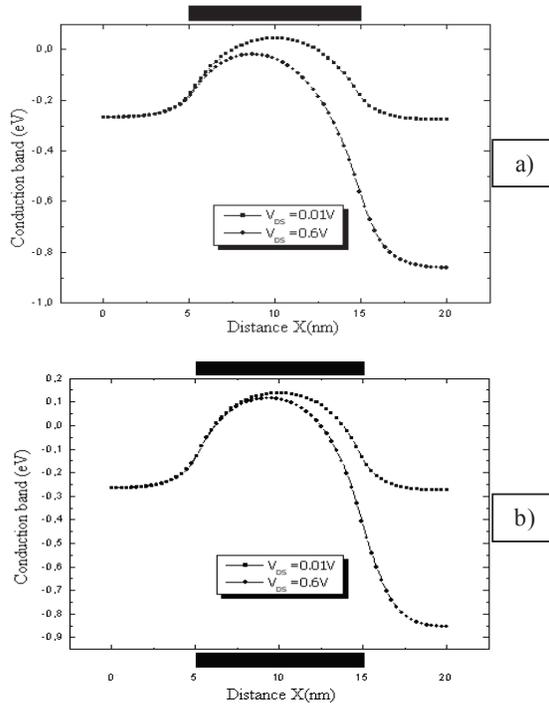
Figure 10. Conduction Band for differences drain voltage of a) Single gate and b) DGMOS.

In this section and the previous one, a comparison was achieved between a single gate and double gate transistor, to highlight that the transistor DGMOS gives better control of the channel compared to the single gate when decreases the thickness T_{Si}. This is summarized in the following table:

TABLE 1. COMPARISON ELECTRICAL CHARACTERISTIC BETWEEN SINGLE AND DOUBLE GATE TRANSISTORS

Thickness	T_{Si}= 1.5nm		T_{Si}= 2nm	
Architectures	SOI	DGMOS	SOI	DGMOS
Saturation Current (I_{ON}) (μA)	1485	1851	2150	2745
Leakage Current (I_{OFF}) (μA)	0.94	0.0043	27.37	0.18
Subthreshold slope (S) (mV/dec)	97	67	158	73
DIBL Effect (mV/V)	178	51	274	78