Analytical Surface Potential Model for Columnar Nanocrystalline Silicon Ultra-Thin Film Transistors

Rachid FATES, Hachemi BOURIDAH and Riad REMMOUCHE
LEM Laboratory, Jijel University
Department of Electronic, Jijel University
B.P. 98, Ouled Aissa, Jijel 18000, Algeria
rachid.fates@yahoo.fr

***Abstract*—An analytical model to calculate the nano-crystalline silicon (nc-Si) ultra-thin film transistors (UTFT) surface potential is proposed. This pattern repose on an ultra-thin channel with a columnar morphology. Our approach is based on the charge trapping at the grain boundary, the well-defined charge distribution into the inversion layer, and the consideration of quantum size effects on dielectric constant and band gap. Results denote that, the surface potential is associated to the silicon crystallites size and geometry. The comparison of our results with existing research model shows a good agreement between the surface potential shapes, and an interesting difference in the surface potential variation, caused essentially by the morphology considered.**

Keywords—nanocrystalline silicon; thin film transistor; quantum size effects; columnar morphology; surface potential;

I. INTRODUCTION

The evolution in materials and process fabrication technologies is posing new challenges in large area nanoelectronics and optoelectronics. The driving force in this evolution is the silicon ultra-thin film technology.

The production of the nc-Si thin films have been under development since a few years ago. Nc-Si is a compromise solution between amorphous silicon (a-Si) and poly-crystalline silicon (poly-Si). The nc-Si films are promising material for the fabrication of Si based TFT [1-4], due to its better electrical stability and higher mobility when compared with its amorphous counterpart, which can be found in a variety of electronic applications [5, 6]. However, the nano-structural properties of nc-Si films are important issues for this technology. The consideration of nc-Si structure for circuit design and simulation is important for electrical and electronic behavior description of the device.

The research in this area is more condensed on the current-voltage relationships, so, several authors have made a considerable study concerning the surface potential for poly-Si TFTs [7-11]. However, a few researches has focused on the study of the nc-Si TFTs electrical characteristics. L.F. Mao [12] has studied the impact of quantum size effects on the dielectric constant and the band gap on the surface potential of nc-Si TFTs, without considering the channel morphology.

Experimental researches have been focused on ultra-thin silicon films in order to determine the crystallites shapes [13]. It has clearly found that the crystallites morphology is columnar, i.e. the columns were formed parallel to the growth direction.

The purpose of this work is to propose a new approach in order to define the surface potential analytical calculation, by considering a columnar crystallites structure, defined by an accurate crystallites size and geometry.

II. SURFACE POTENTIAL MODEL

We present in Fig. 1 an UTFT channel three-dimensional description with a columnar morphology characterized by nanometric crystallites sizes, i.e. crystallites diameter. We consider the silicon nanocrystallites as a set of grains, separated from each other's by an amorphous region (grain boundary).

We assume that in the inversion layer (represented by the dark region into the channel), the grain boundary adjacent electrons are trapped therein, which causes the depletion region formation. Then, by applying Gauss's theorem to the depletion region, the following equation can be derived from the quasi-2D Poisson's equation [14-18]:

$$\varepsilon_{Si}\int_0^{X_d}\frac{\partial\psi(x,y)}{\partial y}dx + C_{ox}\int_0^{y}\left[V_{gs}-V_{fb}-\psi(0,y)\right]dy = qN_aX_d y \qquad (1)$$

where $\psi(x,y)$ is the electrostatic potential, V_{gs} is the gate-source voltage, V_{fb} is the flatband voltage, N_a is the p-type channel doping concentration, X_d is the grain depletion charge depth, C_{ox} is the gate oxide capacitance (ε_{ox}/t_{ox}) where t_{ox} is the gate oxide thickness, and ε_{ox} and ε_{Si} are the permittivity of silicon-oxide and silicon, respectively. We assume that the electrostatic potential has a parabolic distribution with x-axis. Therefore:

$$\psi(x,y)=\psi(0,y)\left(1-\frac{x}{X_d}\right)^2. \qquad (2)$$

Replacing (2) into (1), differentiating both sides with respect to y, and with some algebraic manipulations, (1) becomes:

$$\frac{\partial^2 \psi(0,y)}{\partial y^2} - \left(\frac{3C_{ox}}{\varepsilon_{si} X_d}\right)\psi(0,y) = -\left(\frac{3C_{ox}}{\varepsilon_{Si} X_d}\right)\left(V_{gs} - V_{fb}\right) + \frac{3qN_a}{\varepsilon_{Si}}. \quad (3)$$

The grain depletion charge depth X_d, can be determined from the 1D Poisson's equation. It is expressed as:

$$X_d = \left(\frac{2\varepsilon_{Si}\psi_{S0}}{qN_a}\right)^{0.5} \quad (4)$$

where ψ_{S0} is the potential at (0,0), given by [14, 19]:

$$\psi_{S0} = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right) + \frac{E_i - E_v - \chi_0}{q} \quad (5)$$

where E_i is the intrinsic level, E_v is the valence level, n_i is the intrinsic concentration and χ_0 is determined from the following expression:

$$\left[E_g - \chi_0 - \frac{q^2 N_a}{2\varepsilon_{Si}}\left(\frac{L_g}{2}\right)^2\right]N_D^D + N_D^T E_D^T \exp\left[-\frac{\chi_0}{E_D^T} - \frac{q^2 N_a}{2\varepsilon_{Si} E_D^T}\left(\frac{L_g}{2}\right)^2\right] = N_a L_g \quad (6)$$

where E_g is the band gap, N_D^D is the deep donors states density, E_D^T is the tail donors states level, N_D^T is the tail donors states density, and L_g represents the grain diameter.

Under the following boundaries conditions:

$$\psi(0,0) = \psi_{S0} \quad \text{and} \quad \left.\frac{\partial \psi(0,y)}{\partial y}\right|_{y=0} = 0$$

the solution of (3) represents the electrostatic potential at the grain boundary. It can be expressed as:

$$\psi(0,y) = V_{fb} - \frac{qN_a X_d}{C_{ox}} + \left(\psi_{S0} - V_{gs} + V_{fb} + \frac{qN_a X_d}{C_{ox}}\right)\cosh\left[\left(\frac{3C_{ox}}{\varepsilon_{Si} X_d}\right)^{0.5} y\right]. \quad (7)$$

We suppose that at the strong inversion and under the charge trapping at the grain boundary, we have a lateral depletion y_d along the y-axis as illustrated in Fig. 1. Then, (7) yields to:

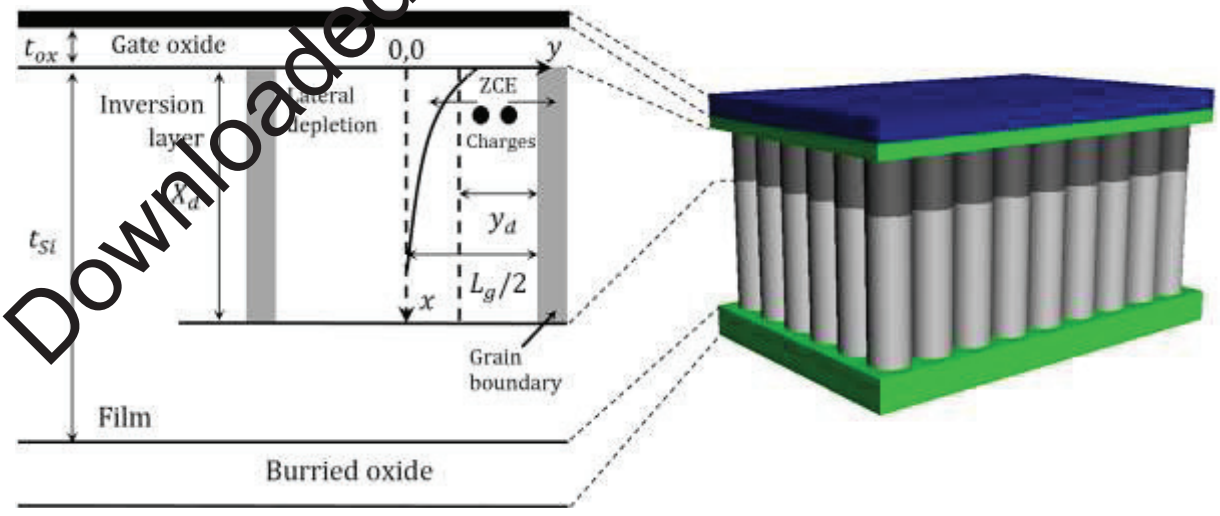


Figure 1. Right, nc-Si TFT ultra-thin channel columnar morphology. Left, channel grain cross section at the strong inversion..

$$\psi_S = V_{gs} - V_{fb} - \frac{qN_a X_d}{C_{ox}} + \left(\psi_{S0} - V_{gs} + V_{fb} + \frac{qN_a X_d}{C_{ox}} \right) \cosh\left[\left(\frac{3C_{ox}}{\varepsilon_{Si} X_d} \right)^{0.5} y_d \right]. \quad (8)$$

This equation shows the surface potential ψ_S at the grain boundary.

Because of the nanometric size of the silicon crystallites forming the channel, the quantum effect must be considered. In low scale, electron-hole pair is confined, this causes the apparition of quantum effects on dielectric constant, ε_{nc-Si}, given by [20, 21]:

$$\varepsilon_{nc-Si}(L_g) = 1 + \frac{10.4}{1 + \left(\frac{1.38}{10^9 L_g} \right)^{1.37}}. \quad (9)$$

The nano-electronic structures have an extremely dependence onto the crystallites size. They can be determined as a function of grain size as follows [22, 23]:

$$\Delta E_g(L_g) = \frac{3.4382}{\left(10^9 L_g\right)} + \frac{1.1483}{\left(10^9 L_g\right)^2}. \quad (10)$$

These both quantum effects, can be included into (8) through the potential ψ_{S0}. So, substituting (9) and (10) into (6), we get:

$$\chi_0 N_D^D - N_D^T E_D^T \exp\left(-\frac{\chi_0}{E_D^T} \right) = \left[E_g + \frac{3.4382}{\left(10^9 L_g\right)} + \frac{1.1483}{\left(10^9 L_g\right)^2} \right] N_D^D - \frac{q^2 N_a N_D^D}{2} \left[1 + \left(\frac{1.38}{10^9 L_g} \right)^{1.37} \right] \times \left[1 + \left(\frac{1.38}{10^9 L_g} \right)^{1.37} + 10.4 \right]^{-1} \left(\frac{L_g}{2} \right)^2 + N_D^T E_D^T \times \exp\left\{ -\frac{q^2 N_a}{2E_D^T} \left(\frac{L_g}{2} \right)^2 \left[1 + \left(\frac{1.38}{10^9 L_g} \right)^{1.37} \right] \right\} \left[1 + 10.4 + \left(\frac{1.38}{10^9 L_g} \right)^{1.37} \right]^{-1} \right\} - N_a L_g \quad (11)$$

χ_0 depends strongly on the both quantum effects on dielectric constant and band gap, it can be determined by solving (11).

It is obvious that there is no analytical solution for (11). To solve this equation, an iterative method has been used. The χ_0 solution can be substituted into (5). Considering (10), we obtain the new ψ_{S0} expression:

$$\psi_{S0} = \frac{kT}{q} \ln\left(\frac{N_a}{n_i} \right) + \frac{E_g}{2q} + \frac{3.4382}{2q\left(10^9 L_g\right)} + \frac{1.1483}{2q\left(10^9 L_g\right)^2} - \frac{\chi_0}{q}. \quad (12)$$

Finally, by replacing (12) into (8), and for $y_d = L_g / 2$ we obtain:

$$\psi_S = V_{gs} - V_{fb} - \frac{qN_a X_d}{C_{ox}} + \left[\frac{kT}{q} \ln\left(\frac{N_a}{n_i} \right) + \frac{E_g}{2q} + \frac{3.4382}{2q\left(10^9 L_g\right)} + \frac{1.1483}{2q\left(10^9 L_g\right)^2} - \frac{\chi_0}{q} - V_{gs} + V_{fb} + \frac{qN_a X_d}{C_{ox}} \right] \cosh\left\{ \left(\frac{3C_{ox}}{4X_d} \right)^{0.5} \left[1 + \left(\frac{1.38}{10^9 L_g} \right)^{1.37} \right]^{0.5} \times \left[1 + \left(\frac{1.38}{10^9 L_g} \right)^{1.37} + 10.4 \right]^{-0.5} L_g \right\}. \quad (13)$$

This final expression shows a new analytical surface potential as a function of the grain diameter, i.e. the surface potential for an UTFT with a nanocrystalline silicon structure described as a range of columnar nanocrystals, separated by amorphous grain boundaries regions. Note that X_d mentioned into (13) becomes:

$$X_d = \frac{1}{q}\left\{\frac{2}{N_a}\left[1+\left(\frac{1.38}{10^9 L_g}\right)^{1.37}\right]^{-1}\left[1+10.4+\left(\frac{1.38}{10^9 L_g}\right)^{1.37}\right]\right\}^{0.5}\left[kT\ln\left(\frac{N_a}{n_i}\right)+\frac{E_g}{2}+\frac{3.4382}{2\left(10^9 L_g\right)}+\frac{1.1483}{2\left(10^9 L_g\right)^2}-\chi_0\right]^{0.5} \quad (14)$$

III. Results and Discussions

We present in Fig. 2 the surface potential variation versus crystallites sizes. The surface potential increases rapidly with a linear form from a crystallite size ~1 nm and reaches a maximum value at ~1 V for a crystallite size ~7 nm. From this crystallite size, the surface potential decreases exponentially and tends to stabilize from a crystallite size ~40 nm.

The evolution of the numerical solution χ_0 of (11) (Fig. 2) shows a strong decay from 5.5 eV to 0.3 eV, when the crystallites size increases in the range of ~1 nm to ~7 nm, due to the influence of the quantum effects on dielectric constant and band gap [20-23]. From a crystallite size of ~7 nm (quantum effects disappearance), χ_0 tends to take a quasi-constant values.

According to Fig. 3, the solutions χ_0 of (11) depend clearly on the both quantum effects on dielectric constant and band gap, since these quantum effects have the same strong variation in the crystallites sizes ranging from 1 nm to 7 nm. i.e. a large decrease for the quantum effect on band gap, from 5.5 eV to 1.5 eV, and large increase for the quantum effect on dielectric constant, from 5.1 to 10.7. For crystallite sizes larger than 7 nm, both quantum effects on dielectric constant and band bap reach to stabilize at ~11.2 and ~1.2 eV respectively. Therefore, we have a quasi-constant values attributed to both effects for the crystallite sizes larger than ~7 nm.

The influence of the both quantum size effects for the crystallite sizes less than ~7 nm is very important. This influence affects significantly the surface potential.

For crystallite sizes larger than ~7 nm, the surface potential values decrease slightly into an exponential. Indeed, the term $\cosh\left(\sqrt{3C_{ox}/4\varepsilon_{nc-Si}X_d}L_g\right)$ in the surface potential expression, becomes dominant.

We compare in Fig. 4(a) our model results with those obtained by L.F. Mao [12]. The model described by L.F. Mao repose onto the consideration of the quantum size effects for a nc-Si TFT, but do not specify the channel morphology, it gives a vague description concerning the channel structure, which is mentioned to be silicon nanocrystals separated by the very thin amorphous grain boundaries.

We present into Fig. 4(b) our model with respect to Mao model with different surface potential axes in order to show the shape comparison. For crystallite sizes ranging from 1 nm to 7 nm, we have a clear difference of ~0.6 V for a crystallite size of 1 nm, which tends to a maximum surface potential difference of ~1.18 V at the peak value corresponding to a crys-

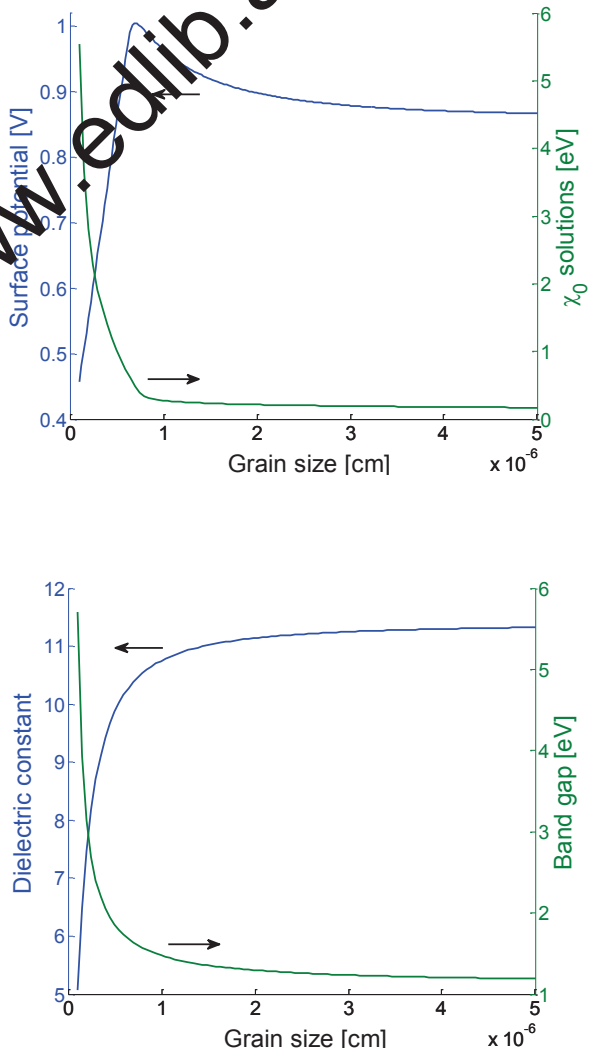
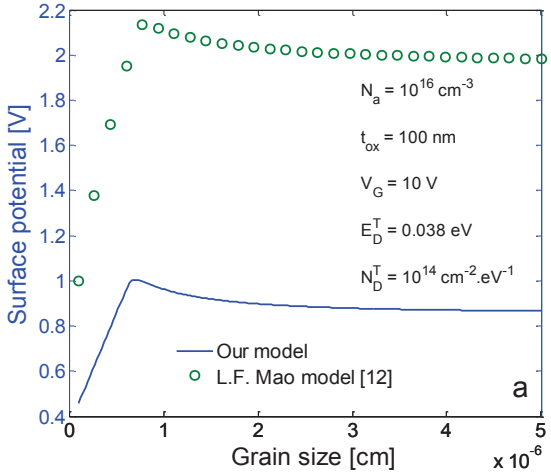


Figure 2. Surface potential and χ_0 solution as function grain size.



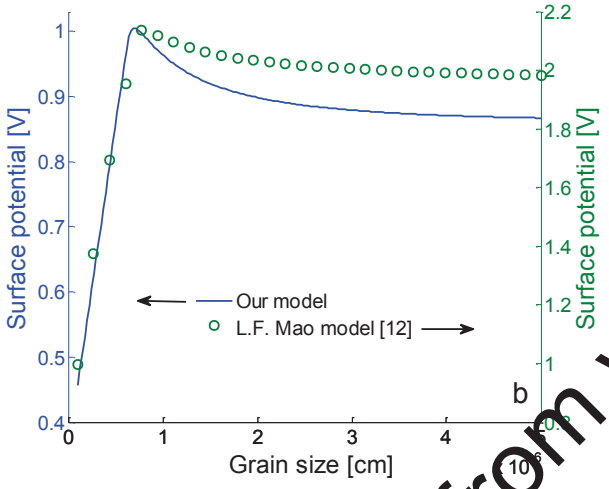


Figure 3. Both quantum size effects on dielectric constant and band gap.

Figure 4. Surface potential versus grain size comparison with L.F. Mao model, (a) same axis and (b) different axis.

tallites size of ~7 nm. A slight difference in the slope is noted in the same range, due to the quantum effects combined with the solutions χ_0 and the hyperbolic cosine. From the crystallites size larger than ~7 nm, we obtain via our model a light exponential decay with respect to the surface potential variation range. This difference highlights the impact of the channel morphology on the surface potential expressed by the term $\cosh\left(\sqrt{3C_{ox}/4\varepsilon_{nc-Si}X_d}\,L_g\right)$, and shows clearly that the channel morphology strongly affects the nc-Si UTFT surface potential.

Basing on these results, we can confirm that our model, which repose on a well-defined channel structure, presents an advantage with respect to L.F. Mao model.

IV. Conclusion

In this work, we have presented an analytical method to calculate the nc-Si UTFT surface potential, by assuming a well-defined channel morphology with a nanometer crystallites size and a columnar crystallites geometry. Results show the effect of the crystallinity in terms of crystallites size and shape on the surface potential. Thus, the quantum effects have a considerable impact on the surface potential especially for small crystallites size. The effect of the crystallites geometry on the surface potential variation has been clearly highlighted, especially for silicon crystallites larger than ~7 nm.

Refrences

[1] T. (Aliyeva) Anutgan, M. Anutgan, I. Atilgan and B. Katircioglu, "Capacitance analyses of hydrogenated nanocrystalline silicon based thin film transistor," Thin Solid Films, vol. 519, pp. 3914-3921, 2011.

[2] I.C. Cheng, S. Wagner and F. Vaillat-Sauvain, "Contact resistance in nanocrystalline silicon thin-film transistors," IEEE T. Electron Dev., vol. 55, pp. 973-977, April 2008.

[3] A.T. Hatzopoulos, N. Arpatzanis, D.H. Tassis, C.A. Dimitriadis, F. Templier, M. Mouchon and G. Kamarinos, "Effect of channel width on the electrical characteristics of amorphous/nanocrystalline silicon bilayer thin-film transistors," IEEE T. Electron Dev., vol. 54, pp. 1265-1269, May 2007.

[4] D. Ocsev, B. Iniguez, L.F. Marsal, J. Pallares and T. Ytterdal, "Device simulations of nanocrystalline silicon thin-film transistors," Solid State Electron., vol. 47, pp. 1917-1920, 2003.

[5] A. Kuo, T.K. Won and J. Kanicki, "Back channel etch chemistry of advanced a-Si:H TFTs," Microelectron. Eng., vol. 88, pp. 207-212, 2011.

[6] Y. Liu, R.h. Yao, B. Li and W.L. Deng, "An analytical model based on surface potential for a-si:h thin-film transistors," J. Disp. Technol., vol. 4, pp. 180-187, June 2008.

[7] W. Deng and J. Huang, "A physics-based approximation for the polysilicon thin-film transistor surface potential," IEEE Electr. Device L., vol. 32, pp. 647-649, May 2011.

[8] R. Chen, X. Zheng, W. Deng and Z. Wu, "A physics-based analytical solution to the surface potential of polysilicon thin film transistors using the Lambert *W* function," Solid State Electron., vol. 51, pp. 975-981, 2007.

[9] P. Migliorato, S.W.B. Tam, O.K.B. Lui and T. Shimoda, "Determination of the surface potential in thin-film transistors from C–V measurements," J. Appl. Phys., vol. 89, pp. 6449-6452, June 2001.

[10] M.J. Siddiqui and S. Qureshi, "Surface-potential-based charge sheet model for the polysilicon thin film transistors without considering kink effect," Microelectr. J., vol. 32, pp. 235-240, 2001.

[11] W. Deng, J. Huang and X. Li, "Surface-potential-based drain current model of polysilicon tfts with gaussian and exponential dos distribution," IEEE T. Electron Dev., vol. 59, pp. 94-100, January 2012.

[12] L.F. Mao, "The quantum size effects on the surface potential of nanocrystalline silicon thin film transistors," Thin Solid Films, vol. 518, pp. 3396-3401, 2010.

[13] Ch. B. Lioutas, N. Vouroutzis, I. Tsiaoussis, N. Frangis, S. Gardelis, and A. G. Nassiopoulou, "Columnar growth of ultra-thin nanocrystalline si films on quartz by low pressure chemical vapor deposition: accurate control of vertical size," Phys. Status Solidi a, vol. 205, pp. 2615-2620, September 2008.

[14] P.S. Lin, J.Y. Guo and C.Y. Wu, "A quasi-two-dimensional analytical model for the turn-on characteristics of poly silicon thin-

film transistors," IEEE T. Electron Dev., vol. 37, pp. 666-674, March 1990.

[15] Y.A. El-Mansy and A.R. Boothroyd, "A simple two-dimensional model for igfet operation in the saturation region," IEEE T. Electron Dev., vol. ED-24, pp. 254-262, March 1977.

[16] C.H. Seager and T.G. Castner, "Zero bias resistance of grain boundaries in neutron transmutation doped polycrystalline silicon," J. Appl. Phys., vol. 49, pp. 3879-3889, July 1978.

[17] S.R. Banna, P.C.H. Chan, P.K. Ko, C.T. Nguyen and M. Chan, "Threshold voltage model for deep submicrometer fully depleted SO1 MOSFET's," IEEE T. Electron Dev., vol. 42, pp. 1949-1955, November 1995.

[18] Z-H. Liu, C. Hu, J-H. Huang, T-Y. Chan, M-C. Jeng, P.K. Ko and Y.C. Cheng, "Threshold voltage model for deep-submicrometer MOSFET's," IEEE T. Electron Dev., vol. 40, pp. 86-95, January 1993.

[19] S.S. Chen, F.C. Shone, J.B. Kuo, "A closed form inversion type polysilicon thin film transistor dc/ac model considering the kink effect," J. Appl. Phys., vol. 77, pp. 1776-1784, February 1995.

[20] L.W. Wang and A. Zunger, "Dielectric constants of silicon quantum dots," Phys. Rev. Lett., vol. 73, pp. 1039-1042, August 1994.

[21] M. Lannoo, C. Delerue, G. Allan and Y-M. Niquet, "Confinement effects and tunnelling through quantum dots," Phil. Trans. R. Soc. Lond. A, vol. 361, pp. 259-273, February 2003.

[22] X. Peng, S. Ganti, P. Sharma, A. Alizadeh, S. Nayak, S. Kumar, "Novel scaling laws for band gaps of quantum dots," J. Comput. Theor. Nanosci., vol. 2, pp. 469-472, September 2005.

[23] A. Zunger and L-W. Wang, "Theory of silicon nanostructures," Appl. Surf. Sci., vol. 102, pp. 350-359, 1996.

Deposition conditions Effect on the structural properties of the polycrystalline silicon films

B. BIROUK

Department of electronics, Technology and science Faculty, Laboratory of renewable energies, University of Jijel, Algeria
Email: bbirouk@univ-jijel.dz

N. DOUKHANE

Department of electronics, Technology and science Faculty, Laboratory of renewable energies, University of Jijel, Algeria
Email: doukhanen@yahoo.com

Abstract-The objective of this work is to study and analyze the properties of the thin films of polysilicon heavily doped with boron, with phosphorus or not doped, deposited by low pressure chemical vapour deposition (LPCVD) from silane (SiH_4) and doping gas (BCl_3, PH_3) on oxidized or not monosilicon substrate, of <111> or <100> orientation. One uses in the analysis of the structural properties of these deposits, the X-rays diffraction (XRD) and scanning electron microscopy (SEM).

The analysis by XRD shows the influence of the substrate orientation and doping level on the grains size of the films. From SEM images one can see the effect of deposit conditions like the temperature and the substrate nature which acts on the grains size and the crystallinity of deposited films, because the particle sizes decrease with the increase in T_d because of the improvement of the high crystallinity of the films with T_d.

Keywords- Polysilicon; X-ray diffraction; images SEM; grains size; crystallinity.

I. INTRODUCTION

The research laboratories were interested these last decades in polycrystalline silicon for into potentialities in microelectronics and photovoltaic applications. It is obtained by deposition in thin layer on the monosilicon substrate or another adapted substrate, at a temperature generally ranging between 550 and 650°C. The structural properties of the deposits are given starting from the analysis by X-rays diffraction (XRD) and the observation by scanning electron microscopy (SEM). These two methods of structural characterization will make it possible to follow the evolution of the crystalline structure of the films according to the deposit conditions, the crystalline orientation of the films as well as the grains size. It should be noted that the samples which are the object of these characterizations, undergo a preliminary cleaning intended to eliminate the oxide coating having grown on the films in contact with the air.

II. PRESENTATION AND ANALYSIS OF EXPERIMENTAL RESULTS

A. Characterization by X-rays diffraction

From the results of the X-rays diffraction (figures 1 to 3), one can say that the grains composing the polysilicon films, crystallize preferentially according to the cristallogarphic direction [111] for the films deposited on a substrate [111], which is in agreement with the literature [1,2,3]. This observation is made on the two types of substrates used in this work: oxidized substrate or not oxidized, and also the doping type of the polycrystalline silicon layers deposited at different temperatures. It is the same for the films deposited on [100] oriented substrate which crystallize preferentially according to the direction [100], as reported in the reference [3].

Another interesting aspect of spectra XRD is the possibility that offers the measurement of widths at half maximum of peaks to estimate the grains size thanks to the formula of Scherrer and al. [1]:

$$FWHM = \frac{Kl}{G\cos\theta}$$

Where $l = 1.54$ Å is the wavelength of the incidental X-rays, G diffracting grains size, θ half of the angle formed by the rays incident and diffracted and K a constant equalizes to 0.9.

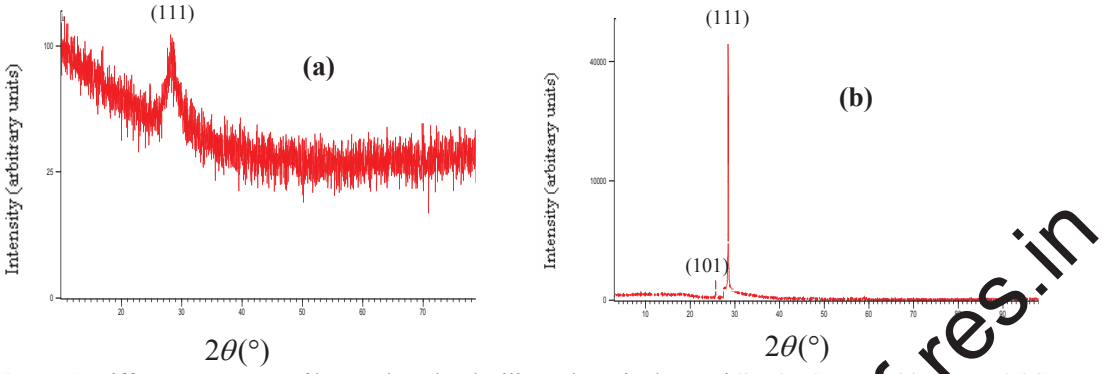


Figure 1. Diffraction spectra of boron doped polysilicon deposited on oxidized substrate: (a) T_d = 570 °C, (b) T_d = 585 °C.

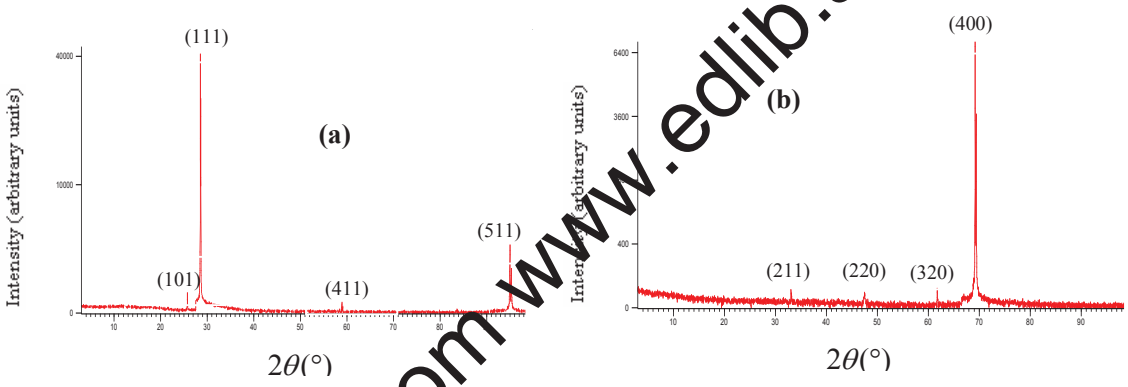


Figure 2. Diffraction spectra of boron doped polysilicon deposited on not oxidized substrate: (a) T_d = 570 °C, (b) T_d = 555 °C.

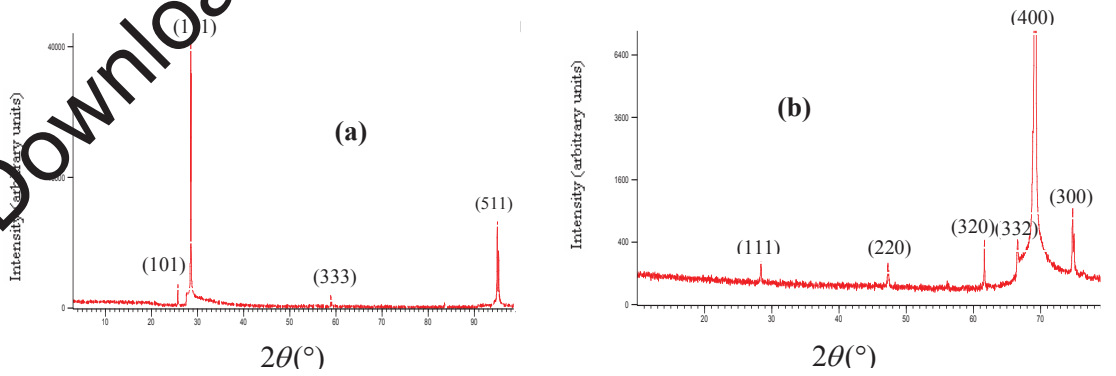
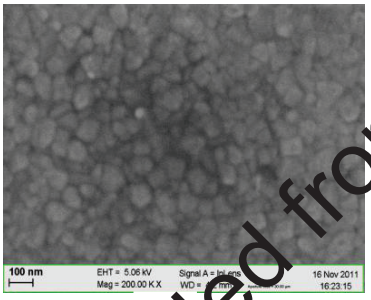


Figure 3. Diffraction spectra of polysilicon deposited on oxidized substrate, (a) undoped deposited at T_d=550, (b) phosphorus doped.

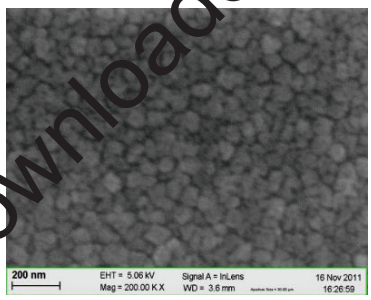
The determination of the grains sizes constituting the polycrystalline silicon films from spectra XRD shows that their size in the case of doping $9x10^{20}$ cm^{-3} is about 1.7 nm, while one leads to 2.8 nm for doping 1. $1x10^{21}$ cm^{-3}. This result shows that the grains size is influenced by doping and increases with the doping concentration. This confirms the results of other work, which showed the influence of doping level on the growth of crystallites. The influence of doping type was also raised in our work. One observes thus that the grains size of films doped with boron is higher than that of grains of films doped with phosphorus. This is explained by the fact that boron reinforces germination and crystallization during the deposition reaction, one can say this impurity tends to promote the silicon deposition. [4]

B. Characterization of polysilicon films by scanning electron microscopy (SEM)

In our study, this method was used to make the topographic images in order to observe the crystallization state of silicon films doped or not with boron, after a cleaning, by means of scanning electron microscope of Philips XL 30 type.



(a)

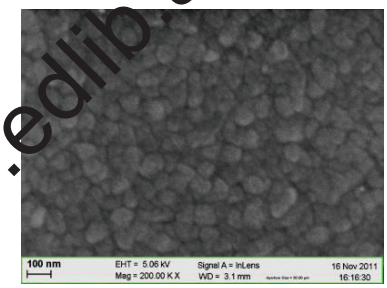


(b)

Figure 4. SEM Observations of the Si-LPCVD films doped with boron ($9x10^{20}$ cm^{-3}): **(a)** deposited on oxidized monosilicon, **(b)** deposited on not xidized monosilicon.

From figures 4, 5 and 6, one notices that crystallinity and texture are shown more clearly in the case of deposited films on not oxidized monosilicon substrate that in case of the deposits on oxide. On these same figures, one observes also a reduction in grains size with increasing deposit temperature, because the grains size of films illustrated in fig.4 (b) and fig.5 (b) is about 86 nm for T_d= 555 °C and 78 nm for T_d= 570. For the films in fig. 4 (a) and fig.5 (a) the measured values are 74 nm and 68 nm, for T_d= 570 °C and T_d= 585 °C, respectively.

(a)



(b)

Figure 5. SEM Observations of the Si-LPCVD films boron doped with a doping level about $10^{21}cm^{-3}$: **(a)** deposited on oxidized monosilicon, **(b)** deposited on not oxidized monosilicon.

This reduction would be related to an increase in the rate of nucleation with T_d where the many and small crystals in the process of growth would prevent the crystals already existing from widening. A low temperature of deposit is synonymous of low nucleation rate and a high grains size. [4, 5]

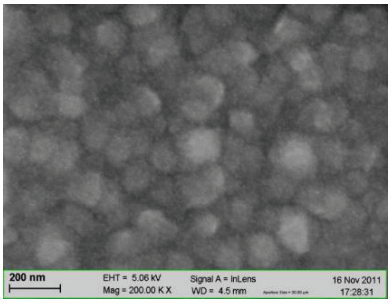


Figure 6. SEM Observation of the undoped Si-LPCVD film deposited on oxidized substrate.

The doping level also influences the grains size since the images show clearly that the grains underwent an increase. Indeed, their mean size increases from 68 nm for the doping level $9x10^{20}$ cm^{-3} (fig. 4(a)) to 74 nm for a higher concentration of doping i.e. $1.4x10^{21}$ cm^{-3} (fig. 5(a)).

As comparison and to measure the layers thicknesses, we carried out transverse SEM observations on the Si-LPCVD films doped with boron and undoped, and deposited on substrates oxidized or not. Figures 7 and 8 show the taken photographs.

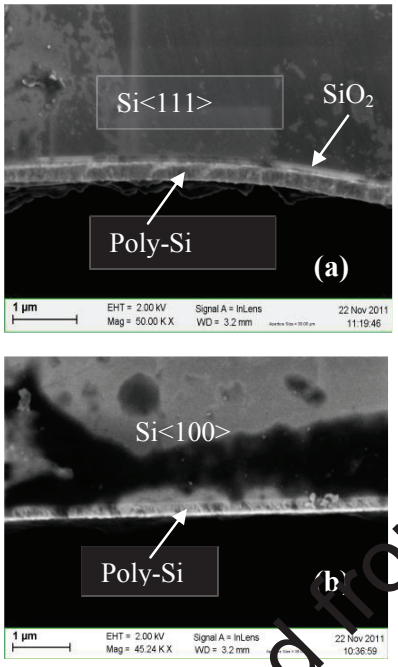


Figure 7. Transverse SEM observations of Si-LPCVD films doped with boron, (a) deposited on oxidized substrate, (b) deposited on bare substrate.

From these figures one observes that all the films, deposited on a substrate oxidized or not, let appear clearly a transverse structure of columnar form. The same report was made elsewhere [6], when the layers are elaborating at similar deposition temperatures. In addition, one observes an increase in the grains size as the thickness of the deposited polysilicon layer increases. These images also allow us to determine the polysilicon layer thickness, which is almost the same one for all the doped films and which one estimate at approximately 2000 Å, while for the undoped film it is about 5000 Å.

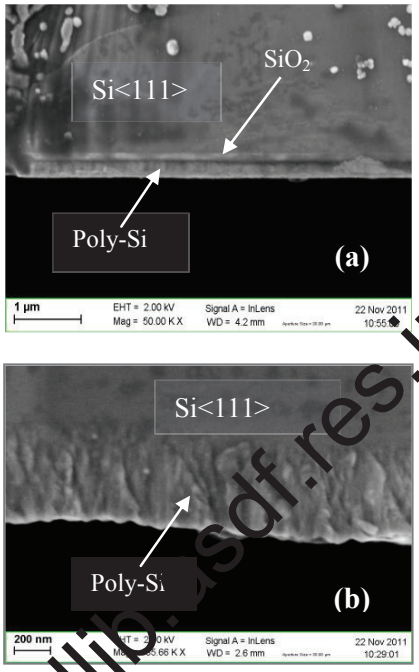


Figure SEM Observations transverse with the Si-LPCVD films, (a) doped film and deposited on oxidized substrate, (b) undoped and deposited on bare substrate.

III. CONCLUSION

In this work, we carried out an experimental study concerning the structural characterization of the polycrystalline silicon films doped with boron or phosphorus or undoped, deposited with low pressure chemical vapour deposition (LPCVD) on monosilicon substrates oxidized or not. These characterizations made it possible to know the crystallographic orientations and the microstructure, such as the shape and the grains size, thanks to the use of X-ray diffraction and SEM observations.

From the results of XRD one can say that the grains composing the polysilicon films crystallize preferentially according to the crystallographic direction of the substrates, in other words <111> and <100>. SEM Images, make it possible to notice that the deposit temperature, the doping level and the substrate nature (oxidized or not), act in an appreciable way on crystallinity like on the grains size. This enables us to say that the characteristics of these deposits are closely related to the deposition conditions.

IV. REFERENCES

[1] S. K. Patil, Z. Çelik-Butler, D. P. Butler, "Piezoresistive polysilicon film obtained by low-temperature aluminum-induced crystallization", Thin Solid Films 519, 2010.
[2] J.R. Heath, S. M. Gates, and C. A. Chess," Nanocrystal seeding: A low temperature route to polycrystalline Si films", American Institute of Physics 1994.
[3] X. Jing, L. Yunfei, Y. Jinling, T. Longjuan, and Y. Fuhua, "Stress and resistivity controls on in situ boron doped LPCVD polysilicon films for high-Q MEMS applications", Journal of Semiconductors, Vol. 30, No. 8, 2009.
[4] B. Birouk, "Study and modeling of the effect of the heat treatments of oxidation dry of the thin films Si-LPCVD strongly doped in-situ with the bore", Doctorate, University of Constantine, 1999.
[5] Y.Laghla, E. Scheid, H.Vernes, J.P.Couderc, "Electronic properties and microstructure of undoped, and B- or P-doped polysilicon deposited by LPCVD", Sol. En. Mat. and Sol. Cells 48, 1997.
[6] N.G.Nakhodkin, T.V. Rodionova, "the mechanism of secondary grain growth in polysilicon films", Journal of Crystal Growth 171, 1997.