Correlation Between Thickness Layer and Grain Size of Polysilicon Layer on Resistivity Behavior: 2D-Numerical Modeling Analysis

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Abstract— **Although many researchers have studied polysilicon thin films in the past several years, there have been few reports on the effects of granular structure on the electrical properties of this layer which becomes increasingly important. The aim of this work is to study the effect of the granular structure on the electrical characteristics of polycrystalline thin film deposited by LPCVD technique, this study have been investigated by a two–dimensional numerical modeling of Poisson's equation based on the finite difference method. The results obtained show good agreement with simulated results**.

Keywords — thickness layer; grain size; polysilicon; resistivity; 2D numerical modeling.

I. INTRODUCTION

The commercial success of active-matrix liquid-crystal displays (AM-LCDs) has stimulated considerable research on thin-film transistors (TFTs), which function as the pixel switches in AM-LCDs. The performance of the TFT depends on the quality of the active layer which can be made of silicon, small-molecule or polymer organics and a few near-ionic compound semiconductors like CdSe. Among these alternatives silicon enjoys a considerable advantage because it draws from a vast technology base [1]. Poly-Si films used in the fabrication of TFTs have been traditionally obtained by solid phase crystallization SPC of as deposited amorphous silicon (a-Si) films, at relatively low crystallization temperatures [2], a low process temperatures (<600°C) also produces numerous defects at the Poly-Si/SiO2 interface and polysilicon boundaries. However, polysilicon materials consist of silicon crystallites (grains) and between them, grain boundaries, i.e. regions with a local potential barrier due to the high density of defects. Quite early it became clear that the polysilicon TFT performance is limited by the granular structure of the channel.

The study of the electrical properties of polycrystalline silicon thin films as a function of granular structure gave rise to many works. Lu and *al* published a systematic study on polycrystalline silicon film resistivity as a function of the film thickness [3] but their study was an analytical modeling.

In this paper a two-dimensional numerical simulation program based on the resolution of Poisson's equation has been used; in our simulation the layer is modeled by a series of monosilicon crystallites, separated by grain boundaries which are perpendicular to polysilicon/oxide interfaces.

We are going to discuss the effect of thickness layer, grain size and number of grain boundaries on the resistivity of polysilicon layer. The effect of Poly-Si active layer thickness and grain size on the activation energy and on the potential barrier have been also investigated for a drain bias equal to 1V.

II. MODELING DESCRIPTION

The structure of polycrystalline silicon is highly dependent on technology used to form the material. When the polycrystalline film is obtained after solid phase crystallization of amorphous silicon film, its structure is columnar. The crystallized material is assumed formed by parallel single-crystalline grains, L_G sized, separated by physically thick amorphous grain boundaries with a thickness of 1 nm.

A. Studied Structure

Fig. 1 shows a schematic cross section of the structure used in our simulation we consider that polysilicon layer is composed of identical grains, the size of which is about L_G 200nm, separated by amorphous grain boundaries with a thickness of 1 nm. We don't take into account the parallel grain boundary since it is far from the upper interface so all the grain boundaries are perpendicular to the growth surface and include the usual density of states (DOS) with exponential band-tails and Gaussian distributed deep levels. More details including the hypotheses and parameters values of the density of states are reported in reference [4].
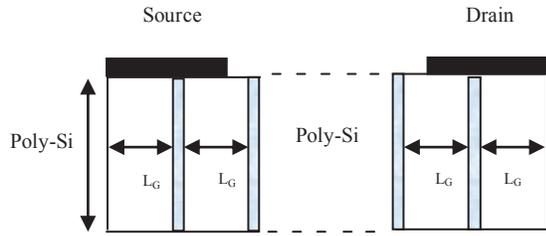
Figure 1. Schematic cross-sectional structure of Poly-Si layer for 2D simulation.

B. Numerical method

The two-dimensional numerical resolution of Poisson's equation for the above described Poly-Si structure is given as:

$$\nabla\big(\varepsilon \mathrm{grad}\Phi(x,y)\big) = -\ q(p(x,y) - n(x,y) + N_D^+ - N_A^- + \sum N_T(x,y)). \tag{1}$$

Used symbols are:
ε : The permittivity of each material;
$n(p)$: The free electrons (holes) density;
Φ: The electrostatic potential;
$N_D^+(N_A^-)$: The ionized donor (acceptor) density;
$\sum N_T$: The sum of the different positively ionized trap centers present in the material.

Partial differential "(1)" is solved by using the finite differences defined by Gummel's decoupling method [5]. For this, the equation is discretized on a variable mesh (strongly refined at interface and grain boundaries) then linearized to first order. The numerical resolution is based on the method of relaxation by line and by column. The tridiagonal character of the matrix leads us to use the Gauss's elimination method.

The resistivity is calculated from the famous relationship linking this amount with the inverse of multiplying of the free carrier concentration and the mobility:

$$\rho = \frac{1}{q \times n_{moy} \times \mu_n}. \tag{2}$$

The mean concentration of electrons in the n-type of Poly-Si layer is calculated from the updating of electrostatic potential in Boltzmann distribution of electrons:

$$n_{moy} = \frac{\int_1^{t_f}\int_1^{Lc} n(x,y)}{\int_1^{t_f}\int_1^{Lc} dx\, dy}. \tag{3}$$

The mobility of electrons μ_n of Poly-Si is given by [6]:

$$\mu_n = \mu_G exp\left(-\frac{q\Phi_B}{kT}\right). \tag{4}$$

Where:
q: The charge of an electron $(1,6\times10^{-19}$ C) ;
n_{moy}: The mean concentration of the electron;
μ_n: The electron mobility;
t_f: Thickness of Poly-Si thin film;
Lc : Channel length of Poly-Si thin film;
μ_G: The mobility of electrons in the monocrystalline grains;
$q\Phi_B$: The potential barrier.

C. Two geometric modeling

- *Two dimensional mesh*

Fig. 2 shows the verification of the mesh used for twenty five grain boundaries which is the maximum points possible retained in programming language. The thickness of the layer is chosen equal to 500 nm while the width is equal to 30µm with a grain size of 200µm, it's clear that the mesh is sufficiently tight at the interfaces and at grain boundaries then it becomes lower heading towards the regions of the crystallites.
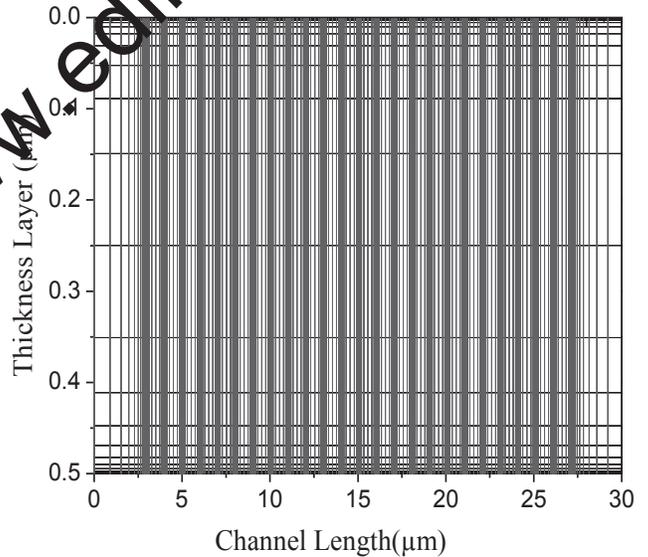
Figure 2. 2D-Mesh of Poly-Si layer.

- *Simulation of Poly-Si layer at thermodynamic equilibrium*

Fig. 3 shows the 2D-plot of electrostatic potential distribution of Poly-Si layer for thickness equal to 150 nm, channel length of 10µm, grain size of 200nm and ten grain boundaries for a less bulky 2D plot. This figure demonstrates the appearance of a height of potential barrier at the grain boundaries with crystallites partially depleted due to the presence of a localized density of intergranular trap.
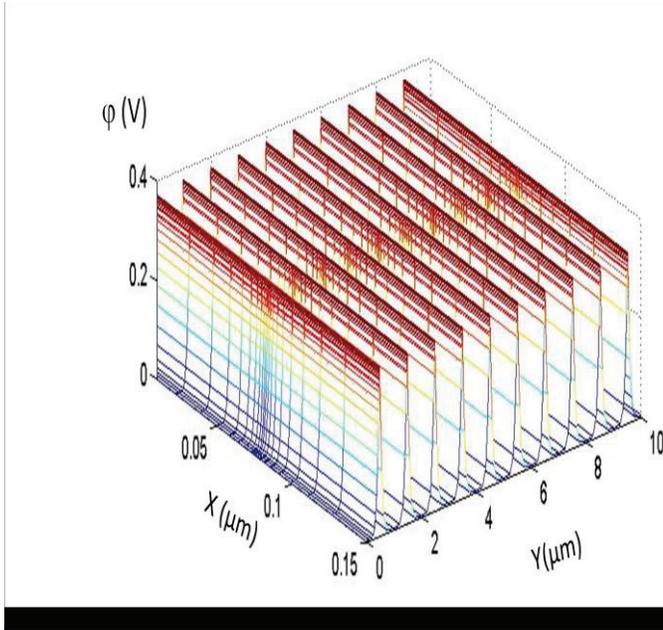
Figure 3. 2D-Distribution of electrostatic potential for ten grain boundaries in n type polysilicon layer.

- *Effect of number of grain boundaries*

Fig. 4 is presented the layer's resistivity of polysilicon in function of doping concentration for different number of grain boundaries. The decrease in the number of grain boundaries in the Poly-Si channel is considered to be accompanied with the growth of the grain size which implies the increase of the crystalline ratio and consequently decrease the resistivity.
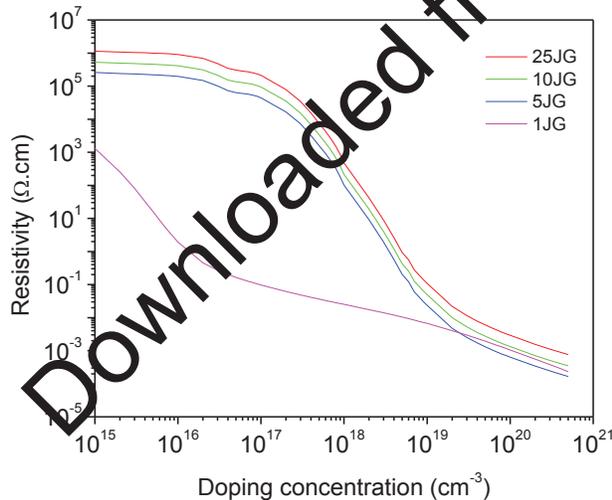
Figure 4. Effect of grain boundaries number on the resistivity of Poly-Si layer.

- *Effect of thickness layer and grain size*

Fig. 5 shows the resistivity of Poly-Si layer as a function of the doping concentration for different values of film thickness and grain size; it can be noticed that when the dopant concentration is more than 10^{17} cm^{-3} the resistivity is much influenced.
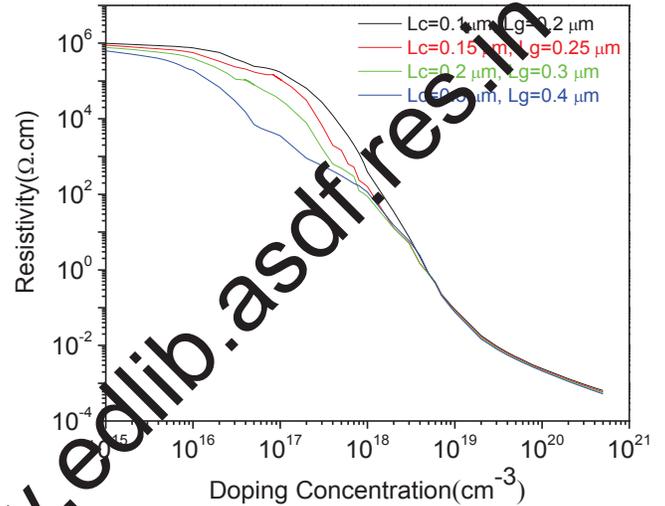
Figure 5. Effect of the couplet layer thickness-grain size on the resistivity of Poly-Si layer.

In Fig. 6, we examined the activation energy ΔEa as a function of the dopant concentration, for several grain sizes L_G and thickness of active layer L_C, it is clear that the activation energy is inversely proportional to the concentration of dopant for all values of active layer thickness and grain size; for a very highly doped layer ΔEa tend to zero.

If grain size and thickness layer are small then there will be more grain boundary present in the channel so the trap state density will be more and a higher channel resistance is expected which results a high activation energy.
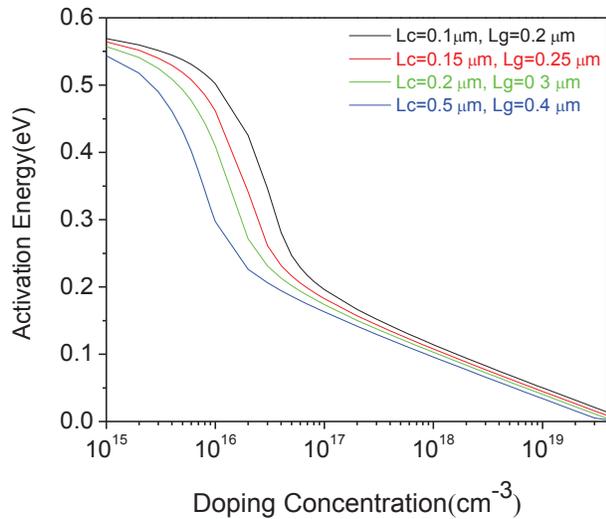
Figure 6. Effect of thinkness layer and grain size on the activation energy.

Fig. 7 shows the behavior of potential barriers as a function of dopant concentration for several film thickness and grain size. The potential barriers resulting from the trapping of charge carriers at the grain boundaries limit the passage of free carriers of a crystallite to another.
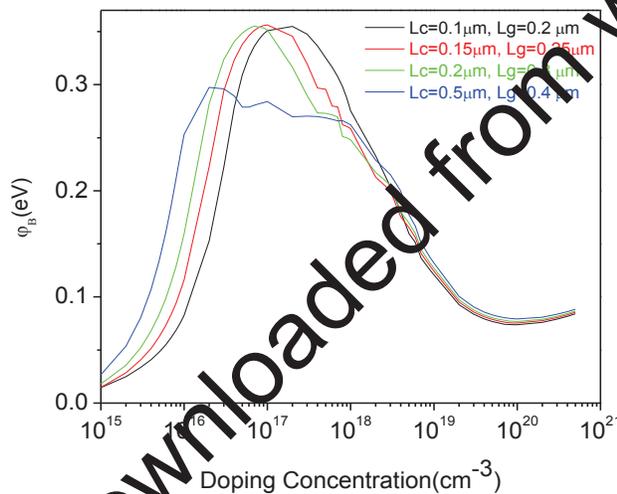
Figure 7. Effect of thinkness layer and grain size on the potential barrier.

CONCLUSIONS

In this paper, a numerical modeling was developed to simulate the effect of granular structure on the electrical characteristic of Poly-Si thin film.
It has been found that:
- A 2D-modeling of the band curvature at the grain boundary allows a good understanding of the evolution of the potential barrier induced by the grain boundary in the channel of a transistor. This potential barrier limits the current through the transistor and decreases the carrier mobility;
- The presence of grain boundaries in Poly-Si layer creates heights potential barriers limiting the passage of free carriers of a crystallite to another;
- The activation energy of a Poly-Si thin film is influenced by the grain size and thickness layer;
- It is a well established fact that electrical properties of polycrystalline films depend on film dimensions.

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