Sine Generator Based on Parallel Cordic

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Abstract— **The field of telecommunications and networks has undergone profound developments and rapid changes in the years 1990. With integration of large public systems, in terms of technology, in particular, transmission networks have seen their abilities increase, particularly regarding the rate supported. The use of field programmable gate array circuits for digital modulation signals has many advantages, particularly the virtually immediate validation features, and an unparalleled facility of adaptation in case of change of protocol or modulation type, however implementation on field programmable gate array makes us dependent and limited by the speed of this type of circuit and the quantity of resources (in the form of elementary cells) available. These limitations can be significantly the algorithms used, and using simple arithmetic functions, that take into account the architectural features of these components. This work presents some techniques that obtains a digital modulation signal, specialy focusing on the quadrature amplitude modulation having the particularity require controlling two parameters of the sine wave output which are phase and amplitude. It is thus one of the most complex modulations used today in passing of protocols. For the implementation on digital circuits, it is necessary to take the sampling as a factor on the highest frequency of the system. In our work we present some technique to obtain a sine wave generator based on a parallel CORDIC processor using -Virtex5 XUPV5-LX110T the platform, and ISE 12.2 software automatically adapts the VHDL type of modulation desired.**

Keywords-coordinate rotation digital computer; field programmable gate array circuit; qam modulation; vhdl ; software ise 12.2;

I. INTRODUCTION

It is not possible on an FPGA-type Virtex5 XC5VLX110T actually available to achieve the sampling frequencies required to the sine wave of high frequency [1, 2, 3]. In our work we game study the iterative implement a CORDIC on this circuit, this architecture requires multiple clock cycles to produce a sample sinusoids. This architecture does not cover sampling frequency to produce the largest possible. The uses of different architecture produce at each clock cycle a sample sinusoid, is the CORDIC angle recoding (pipeline without accumulator) ,and uses the parallel cordic which to allow the production of samples in a shifted way, the last one increases the sampling frequency.

II. Qam Modulator

Quadrature amplitude modulation (QAM) is a modulation scheme in which two sinusoidal carriers, one exactly 90 degrees out of phase with respect to the other, are used to transmit data over a given physical channel. One signal is called the "I" signal, and can be represented by a sine wave. The other is called the "Q" signal, and can be represented by a cosine wave. Because the carriers occupy the same frequency band and differ by a 90-degree phase shift, each can be modulated independently, transmitted over the same frequency band and separated by demodulation at the receiver. For a given bandwidth, QAM enables data transmission at twice the rate of standard pulse amplitude modulation without any degradation in the bit error rate [4, 5]. QAM and its derivatives are used in both mobile radio and satellite communication systems. Each symbol is a specific combination of signal amplitude and phase. By combining the amplitude and phase modulation of a carrier signal, it is possible to increase the number of possible symbols and therefore transmit more bits for each symbol. In fact, the expression of the modulated signal is written like this [6]:

$$S(t) = A(n)\cos(\omega t + \phi) - B(n)\sin(\omega t + \phi). \quad (1)$$

$$S(t) = | A(n) + jB(n)\exp j\omega t + \theta |. \quad (2)$$

III. ARCHITECTURE OF THE DIGITAL MODULATION QAM

A digital modulator is composed of four main parts which are the phase accumulator, sine generator, encoder, digital and analog low-pass filter [7].

IV. SINE GENERATOR BASED OF CORDIC PROCESSOR

A. Cordic Arithmetic

CORDIC acronym Coordinate Rotation DIgital Computer is an algorithm for calculating trigonometric and hyperbolic functions, including use in calculators [8]. It was first time in 1959 by Jack E. Volder. It looks like techniques that were described by Henry Briggs in 1624 [9, 10].

B. Principe of Cordic Processor

The principle of the CORDIC algorithm as described by Volder, is relatively simple [11, 12]. Its role to effect the matrix rotation angle of the vector $\vec{V}\binom{0}{1}$ of the unit circle, like rotation can be written in the following form:

$$\overrightarrow{V'} = \begin{pmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{pmatrix} \cdot \vec{V} \cdot \quad (3)$$

By placing cos θ factor, this may also be written

$$\overrightarrow{V'} = \cos\theta \begin{pmatrix} 1 & -\mathrm{tg}\theta \\ \mathrm{tg}\theta & 1 \end{pmatrix} \cdot \vec{V} \cdot \quad (4)$$

In fact, for a value of θ taken in the interval $]-\frac{\pi}{2};\frac{\pi}{2}[$, Volder has shown that there a sequence of values d_i exists, d_i with $\epsilon \{-1,1\}$, for which $\theta = \sum_{i=0}^{\infty} d_i \arctan 2^{-i}$ Thus, a rotation angle θ can be written in the following matrix form [13,14]:

$$\overrightarrow{V'} = \prod_{i=0}^{\infty}(d_i \cdot \mathrm{arctg}2^{-i}) \cdot \prod_{i=0}^{\infty} \begin{pmatrix} 1 & -d_i 2^{-i} \\ d_i 2^{-i} & 1 \end{pmatrix} \cdot \overrightarrow{V}. \quad (5)$$

To simplify this expression, we can pose:

$$C_\infty = \prod_{i=0}^{\infty} \cos(d_i \mathrm{arctg}2^{-i}) = \prod_{i=0}^{\infty} \cos(\mathrm{arctg}2^{-i}) \cdot \quad (6)$$

Because the function cos is pair ≈ 0.6073.

C. Operating Mode of Cordic Processor

Following its mode of operation, the CORDIC can be to used for different purposes. You can:

-Or know the angle of a vector M(x,y)
Mode VECRORING.

- Or ask him to perform the rotation of a vector by an angle θ
Mode ROTATION.

In the latter mode, with values x and y, the functionalities, we can also obtain the values of sinθ and cosθ [15].

TABLE I. THE OPERATING MODES OF THE CORDIC

Mode	Pre-Conditions	Post-Conditions	Sense of Progression
Rotation	$x_0 = x$ $y_0 = y$ $z_0 = \theta$	$x = x^* \cos\theta - y^* \sin\theta$ $y = y^* \cos\theta + x^* \sin\theta$ $z = 0$	$d_i = \begin{cases} -1 & \text{si } z_i < 0 \\ +1 & \text{or else} \end{cases}$
	$x_0 = 0$ $y_0 = 1$ $z_0 = \theta$	$x = -y^* \sin\theta$ $y = x^* \sin\theta$ $z = 0$	
Vectoring	$x_0 = x$ $y_0 = y$ $z_0 = 0$	$x = 0$ $y = \sqrt{x^2 + y^2}$ $z = \tan^{-1}(\frac{y}{x})$	$d_i = \begin{cases} -1 & \text{si } x_i < 0 \\ +1 & \text{or else} \end{cases}$

V. ARCHITECTURE OF CORDIC PROCESSOR

The different architectures cordic processor

A. Architecture iterative cordic

This architecture is used for generating digital sine it is composed of three main elements [16,17]:

- a read only memory (Rom), containing pre-calculated values of arctan 2^{-k}.
- a combinational block, loaded for calculating successive values of x_k and y_k.
- a combinational block, loaded for evaluating the remaining angle.

$\overrightarrow{V_k}\begin{pmatrix} x_k \\ y_k \end{pmatrix}$ is the vector obtained in the k^{th} iteration, the micro-rotation for rotation $\overrightarrow{v_k}$ to $\overrightarrow{v'_k}$ is equivalent to the system:

$$\begin{cases} x_{k+1} = x_k - y_k d_k 2^{-k}. \\ y_{k+1} = y_k + x_k d_k 2^{-k}. \\ z_{k+1} = z_k - d_k arctg2^{-k}. \\ d_{k+1} = -1 \; si \; z_{k+1} \geq 0{,}1 \; or \; else. \end{cases} \quad (7)$$

C_N corresponding to an error made on the value $\overrightarrow{V'}$ of the vector $\vec{V}$ resulting, but this value, called scale factor, depond not the number of performed micro-rotations, and not their sense. On choosing a vector $\vec{V}$ like that $\overrightarrow{V}\begin{pmatrix} A.C_N \\ 0 \end{pmatrix}$.

At the beginning of operation of the circuit, the blocks X and Y are pre-loaded with the values 0 and A • C_N respectively, and Z is loaded with the value of the angle whose cosine is to be calculated, namely Θ. At every iteration, the new values of X and Y are calculated based on the values of the preceding step, and the direction of rotation given by the sign of Z.

The value of Z is changed to reflect the rotation that it rest to make of affect the rotation angle Θ. The calculation is terminated when Z = 0, to the accuracy close to the circuit architecture on which this is implanted. It takes about n+1 iterations to get the value of a sine wave sample with a precision of n bits.

B. Architecture pipeline cordic without accumulator

For a theoretical precision of n bits, there are (n +1) stages [18, 19]. Either pipeline stage is not loaded of effect that a single micro-rotation always the same, the k^{th} stage corresponds to the system of equations [20, 21, 22]:

$$\begin{cases} x_{k+1} = x_k - y_k d_k 2^{-k}. \\ y_{k+1} = y_k + x_k \cdot d_k 2^{-k}. \\ \alpha_0 = \sum_{k=1}^{\infty} 2^{-k}. \\ \theta = \alpha_0 + \sum_{k=1}^{\infty} c_k 2^{-k}. \end{cases} \quad (8)$$

This architecture allows the circuit which it is implemented to achieve higher clock frequency that obtained with other

algorithms presented, because it reduces the critical path of the combinatorial portion of each pipeline stages by removing the sign detection stage, and one of the adders / subtractors.

It uses:

- N +1 adder subtractor complete paths for each of the three calculations (X, Y, Z).
- 2 (N +1) shifts, requiring no combinational logic element.

C. Architecture Parallel Cordic

The principle of this structure is presented on allowing the production of samples in a shifted way, it is necessary to modify the provided term of phase in a following way.

$$\emptyset' = w.T_e\,(m.\,n+i) + \Phi(n). \qquad (9)$$

VI. IMPLEMENTATION AND RESULTS

Different architectures are implemented on a circuit FPGA (XC5VLX110T).The software tools used for this synthesis are ISE12.2. This software ISE12.2 is an integrated environment (company Xilinx) development of digital systems on reconfigurable components with purpose a hardware implementation on FPGA. ISE is available at www.xilinx.com in divers versions (..., 8.1, 9.2, ... 10.1, 12.2, 12.3 ...).In ISE, the design can be described in three main forms:

-Diagrams,

- hardware description language (HDL) like as VHDL, Verilog,etc....

-State Diagrams.

A. description language VHDL

VHDL is the VHSIC Hardware Description Language. VHSIC is an abbreviation for Very High Speed Integrated Circuit. It can describe the behaviour and structure of electronic systems, but is particularly used as a language to describe the structure and behaviour of digital electronic hardware designs, such as ASICs and FPGAs as well as conventional digital circuits.

B. Synthesis results

TABLE II. COMPARISON TABLE BETWEEN ITERATIVE CORDIC AND PIPELINE CORDIC WITHOUT ACCUMULATOR.

Architectures / n(bits)	Iterative Cordic			Cordic With Recoding		
	Frequency Maximum (M-Hertz)	*Frequency on sampling (M-Sample/s)*	*Cells (cell)*	*Frequency Maximum (M-Hertz)*	*Frequency on sampling (M-Sample/s)*	*Cells (cell)*
08	378.458	47.307	106	422.518	107.804	136
16	354.070	22.129	208	549.768	66.625	465
32	339.929	10.622	415	455.154	10.965	1953

TABLE III. THE RESULTS OF PARRALEL CORDIC.

Architecture / n(bits)	Parallel Cordic		
	Frequency Maximum (M-Hertz)	*Frequency on sampling (M-Sample/s)*	*Cells (cellule)*
08	2410.072	431.216	544
16	2199.072	266.5	1860
32	1820.616	43.86	7812

C. Synthesis Results on 8 bits

- **Modes**

Diagrammatic

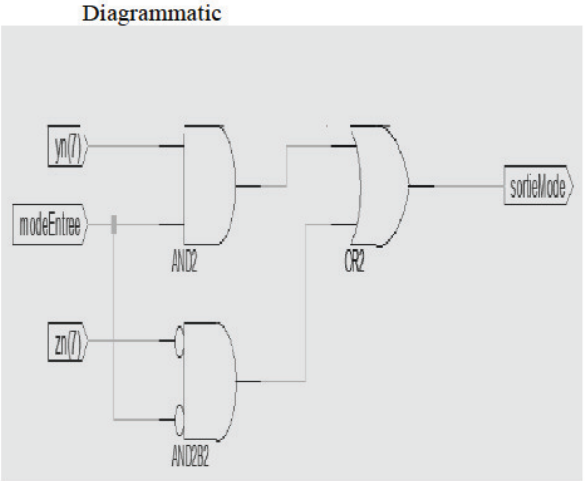


Figure 1. The diagrammatic modes of the CORDIC processor.

Technological

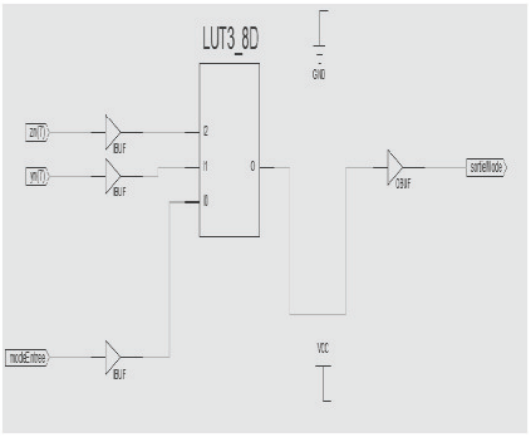


Figure 2. The technological ode o f the CORDIC processor.

Test bench

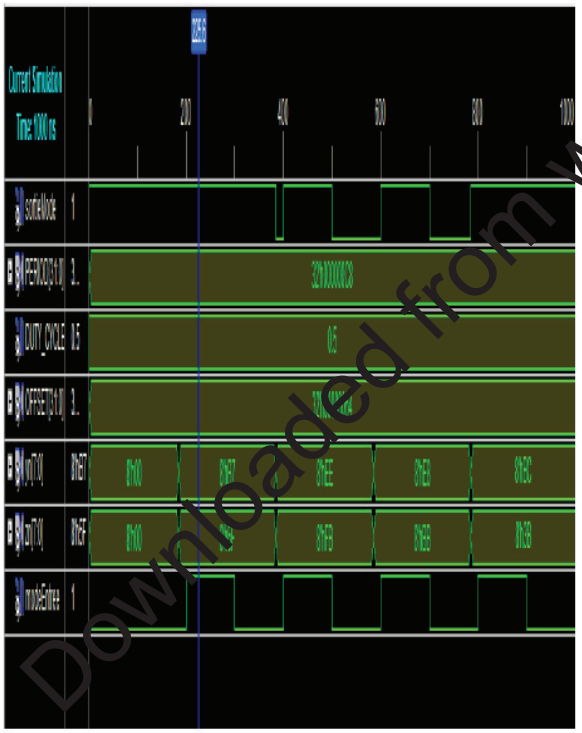
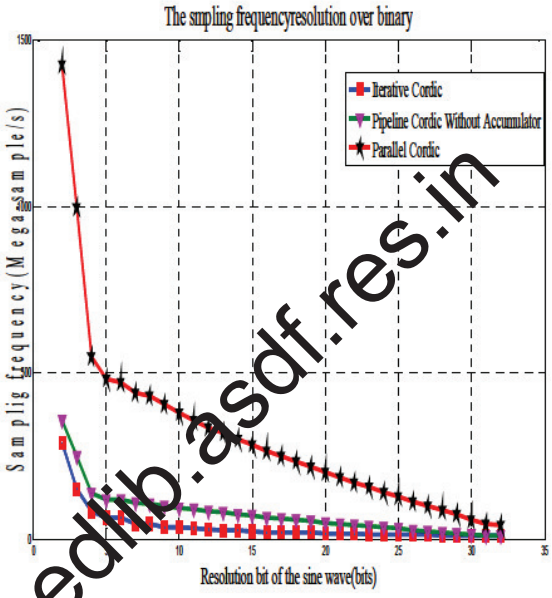


Figure 3. Tes bench of the CORDIC processor.

D. The sampling fre uency compared the other structure



Figu . .Maxi u am ling ate reached with various architectures.

In The different bits we achieve better frequency sampling tructure of generator si s id based parallel CORDIC because produce at either clock cycle a sample of sine ut the her ar itecture requires divers clock cycle to produce a sample. T s is not suitable for producing a sampling frequency la g as possible.

E. The number of cells s a function of binary resolution

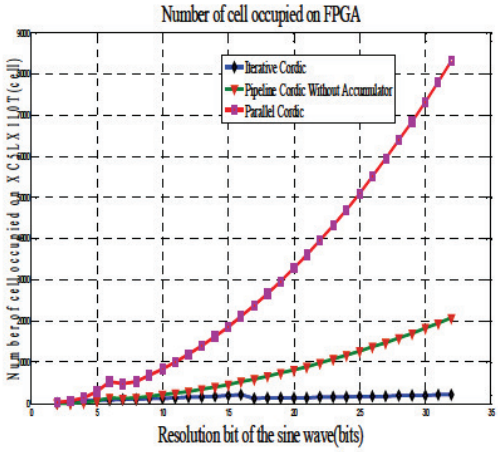


Figure4. Number o ogi c lls used on the FPGA XC5VLX110T.

We will see in the resul s of the three implementations on FPGA structure parallel ORDIC uses several numbers but

the iterative and recoding angle CORDIC uses minimum number of cells.

F. The number of cells as a function of sample frequency

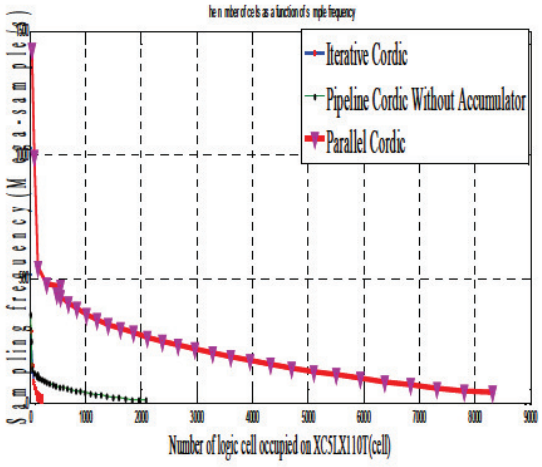


Figure 5. Sampling frequency depending on the number of logic cells occupied.

In both curves we will see structure is based iterative CORDIC uses minimum sampling frequency and the number of cells, this is bad architecture because requires several clock cycle to produce a sample. We develop this structure to simply remove the accumulator of angle each clock cycle, which produce a sample of this sine and use parallel cordic is presented on allowing the production of samples in a shifted way, last increased the sampling frequency for the purpose of this work which we wish.

VII. CONCLUSION

We presented in this section an architecture of generation of sine wave using a processor CORDIC to fulfill the requirements of an optimal establishment on a digital circuit of type FPGA XC5LX110T. The resulting structure authorizes the effective use of a pipeline, which makes it possible to obtain a short critical path and thus a frequency of operation of more important circuit FPGA. Lastly, the simplification of the algorithm by the removal of the accumulating stage of angle, makes it possible to reduce occupied surface, and. This last architecture multiplies the number of samples actually produced in only one cycle of clock, and use structure parallel cordic for increases sample of this sine by as much the effectiveness of modulator QAM.

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