Electrical Characteristics Comparison Between Single Gate SOI N- MOSFET And Double Gate SOI N-MOSFET Using Silvaco Software

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Abstract— **Investigation of electrical characteristics of single gate SOI MOSFET and double gate DG SOI MOSFET devices in order to compare their electrical characteristics using Silvaco software was done and presented in this paper. The comparisons were focused on four main electrical characteristics that are threshold voltage, saturation current, leakage current and subthreshold voltage. The device structures and the characteristics were constructed, examined and simulated using Silvaco-Atlas.Results were analyzed and presented to show that the electrical characteristics of DGMOSFET transistor are better than that SOI MOSFET transistor.**

Keywords-Technology SOI, SOI MOSFET, DG SOI MOSFET, Silvaco Software.

I. INTRODUCTION

The CMOS transistor gate length scaling is projected to continue through 2016 down to the incredible 9 nm [1, 2].

Even if these dimensions can be realized using technological innovations, CMOS devices will suffer from a number of short channel effects, such as the threshold voltage roll-off, the drain induced barrier lowering (DIBL) and the subthreshold swing all of which degrade the MOSFET performance.

A number of solutions have been proposed to overcome these problems [1, 3]. Employing SOI technology gives a good alternative to that miniaturization. SOI technology allows the reduction of short channel effects that appear in nanometer devices (under 50nm node) and also allows micro-electronic evolution to continue.

New architectures using SOI MOSFETs had been very seriously considered to replace bulk MOSFET architecture.

The double-gate SOI MOSFET is considered as a promising device for CMOS scaling to deep sub-100 nm, gate lengths has become very attractive for scaling CMOS devices down to nanometer size [4].Double gate allows for higher current drive capability compared with single gate SOI MOSFET and lower output conductance for analog applications [4].

II. SOI DEVICES FOR THE NANOMETRIC LENGTH

The Silicon-On-Insulator technology is a viable alternative to the mainstream Bulk architecture for the next technology nodes. In a SOI wafer the silicon active region, where devices are patterned, is separated from the substrate by a thick oxide region. These include **S**eparation by **I**mplantation **O**f **OX**ygen (SIMOX) [5], **Z**one **M**elting **R**ecrystallization (ZMR) [6], **F**ull **I**solation by **P**orous **O**xidized **S**ilicon (FIPOS) [7], and **W**afer **B**onding (WB) [8]. In the second group, the semiconductor film is deposited directly onto an insulating substrate. This is the case for **S**ilicon **O**n **S**apphire (SOS) [9], and **S**ilicon **O**n **Z**irconia (SOZ) [10].

Compared to bulk, the basic characteristic of SOI technology is the separation of the top active region from the underlying mechanical substrate by a thick insulator layer (Fig. 1). This difference leads to some advantages over bulk silicon [11].

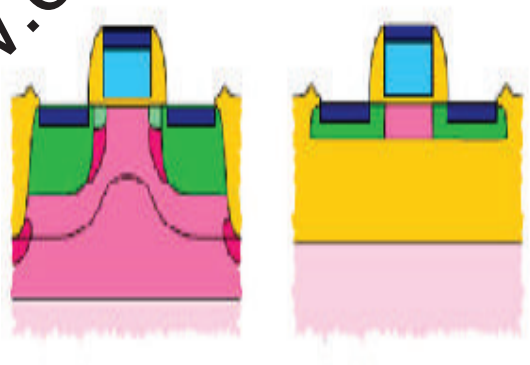

Figure 1. Cross-section of a bulk and a SOI MOSFET. The SOI device is separated from the mechanical substrate by an insulating layer [12].

The main differences with the standard MOS of Fig.1 are:

- The vertical isolation protects the active region from many parasitic effects like radiation-induced photo-currents and latch-up;
- The isolation reduces the parasitic capacitances and leakage currents of the pn junctions.
- The lateral inter–device isolation in the SOI case does not need trenches or well formation;

Starting from an SOI wafer, many different types of MOS transistor can be obtained. The first classification is between the Single-Gate SOI MOSFET and the Multi-Gate SOI MOSFET. While the former has found a commercial application, the latter is still confined in the research area and will be described in a specific subsection.

III. SINGLE-GATE SOI MOSFET

A MOS transistor designed on a SOI wafer has a cross-section like the one in Fig.2.

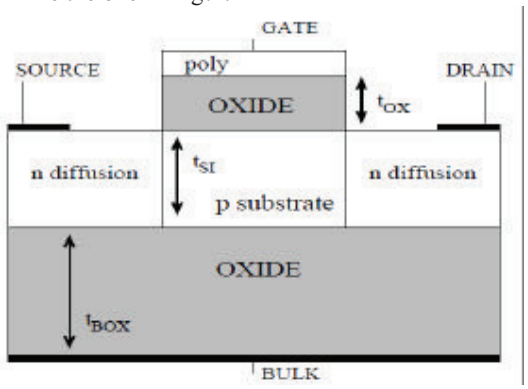

Figure 2. Schematic structure of a Single-Gate SOI MOSFET. A thick back-oxide region separates the active area from the bulk contact, which, for SOI devices only, is often called back-gate contact [16].

Depending on the thickness of the top silicon layer (t_{SI}), Single-Gate SOI MOSFETs can be further classified into two categories [13]:

- ***Partially-Depleted (PD)*:** if the active silicon body is thick enough to contain completely the depletion region in strong inversion.
- ***Fully-Depleted (FD)*:** if the fin thickness t_{SI} is so thin that the depletion region touches the bottom of the silicon body. Also the depths of the source and drain diffusions are limited by t_{SI} .

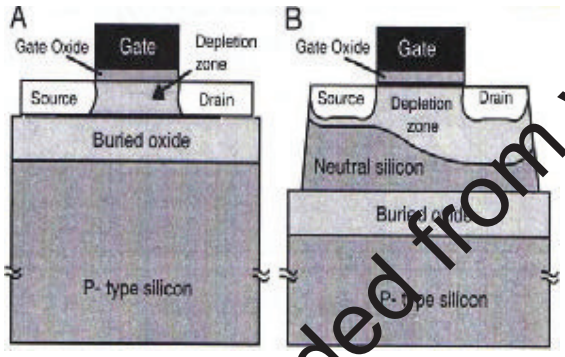

Figure 3. (A) - Fully depleted SOI MOSFET, (B) -Partially depleted SOI MOSFET [14].

When the SOI process was presented [13], its higher cost limited its diffusion to the applications where radiation hardness was a main problem. With the continuous technological development the IC designers were founding increasing issues in parasitic control and power consumptions. At the same time the research on SOI technology has increased exponentially and SOI has become an interesting alternative to the standard devices because of the reduced parasitic effects.

At the moment all the integrated circuits on SOI wafers use the Partially- Depleted structure because the technological process to create a "thick" body is much easier. The design rules of a PD-SOI MOS transistor are not very different from the bulk case and the scaling rules are almost the same, for example the doping concentration of the body must be increased while decreasing the gate length L_G to control the SCE.

On the contrary the FD-SOI MOSFET is quite different from the bulk transistor .The FD concept is applied not only to Single-Gate but also to Multiple Gates devices.

IV. DOUBLE-GATE MOSFETS

The advancement in the MOS technology has allowed the creation of devices with multiple gate contacts, like the Double-Gate MOSFET or the Trigate [13]. All these devices take advantage of the fully-depleted behavior. Thanks to the combination of thin t_{SI} and multiple gate contacts, the control of the body by the gate voltage is greatly enhanced and the short-channel effects are reduced in comparison with single-gate devices. The Double-Gate SOI MOSFET is the most common example of multi-gate transistor and the research about it has increased in the last years.

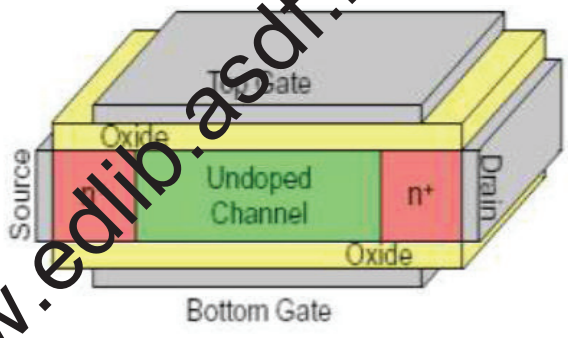

Figure 4. A Schematic diagram of Double Gate SOI MOSFET [15]

The DG SOI MOSFET is of the same material as the bulk MOSFET, i.e., silicon, but has a different structure. It offers better control of short-channel effects (SCE) control [16] arising from the use of two gates with an ultra-thin body (UTB); and high drive current per device width resulting from high mobility due to low transverse electric field and higher inversion carrier density from the two channels. The DG SOI MOSFET need not require drastic changes in the existing CMOS process technology. Fig.4 shows a schematic of a DG SOI MOSFET. The thin channel is sandwiched between the two gates, one of which is buried in the SOI island. When the properties of both gates (gate work function, gate oxide thickness, and bias) are identical, the device is called a symmetric double-gate (SDG) MOSFET; otherwise, it is an asymmetric double-gate (ADG) MOSFET. While the electrical characteristics of the channel of the DG SOI MOSFET are promising, high source/drain resistance (RS/D) due to the thin silicon and difficulty in aligning the two gates cloud this device's future [16].

V. DEVICE SIMULATION

Simulations of single gate SOI N- MOSFET and double gate SOI N-MOSFET symmetrical device were performed by the SILVACO TCAD tools [17-18]. Typical values of the various transistors parameters used in these simulations are shown in Table I and Table II.

TABLE I. PARAMETERS OF SINGLE GATE SOI N-MOSFET TRANSISTOR

Symbol	Designation	Value
L_D,L_S	Drain length, and Source length	10[nm]
L_G	Gate length	10[nm]
T_{OX}	Gate oxide thickness	1.5[nm]
T_{BOX}	Buried oxide thickness	1.5[nm]
Tsi	Silicon film thickness	3[nm]
N_A	Substrate concentration	$1x10^{18}$[cm-3]
N_D	Drain and Source concentration	$1x10^{20}$ [cm-3]

TABLE II. PARAMETERS OF DOUBLE GATE SOI N- MOSFET TRANSISTOR

Symbol	Designation	Value
L_D,L_S	Drain length, and Source length	10[nm]
L_G	Gate length	10[nm]
$T_{OXl} = T_{OX2}$	Gate oxide thickness	1 5[nm]
Tsi	Silicon film thickness	3 [nm]
N_A	Substrate concentration	$1x10^{18}$[cm-3]
N_D	Drain and Source concentration	$1x10^{20}$ [cm-3]

Fig.5, Fig.6 illustrates respectively the Device structure of the SOI N- MOSFET and Symmetrical DG SOI N- MOSFET.

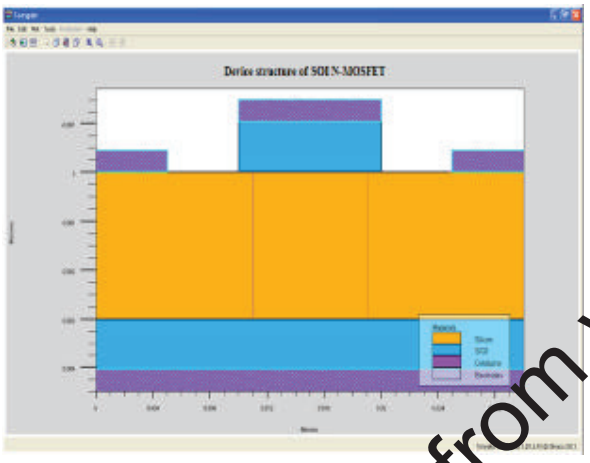

Figure 5. Device structure of the single gate SOI N-MOSFET.

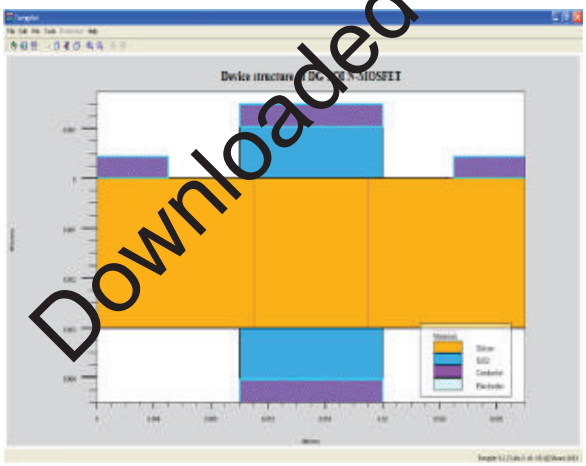

Figure 6. Device structure of the Symmetrical double gate SOI N-MOSFET.

The Fig. 7 represent the output characteristics (I_{DS} /V_{DS}) of SOI N-MOSFET and of DG SOI N-MOSFET transistors with V_{GS}=0.1V

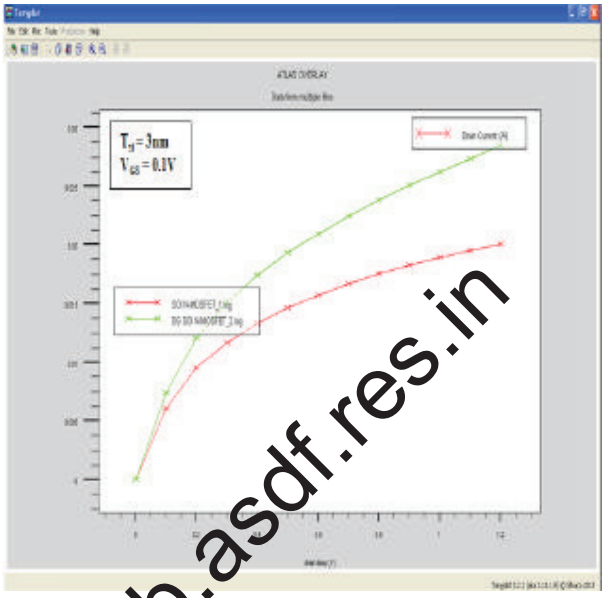

Figure 7. I_{DS}- V_{DS} Characteristics for SOI N-MOSFET and DG SOI N-MOSFET.

From Fig. 8 it is observed that the threshold voltage of DG SOI N-MOSFET is better than those corresponding to SOI N-MOSFET.

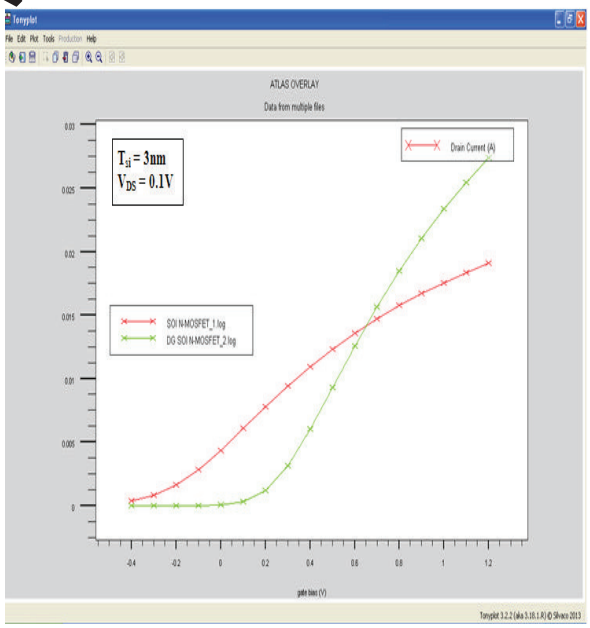

Figure 8. I_{DS}-V_{GS} Characteristics for SOI N-MOSFET and DG SOI N-MOSFET

The saturation current I_{DSAT} east liked significant in the DG SOI N-MOS compared to the SOI N-MOSFET transistor.

The leakage current output is I_{DS}_leakage=0.0181533A in SOI N-MOSFET and I_{DS} _leakage=0.00119583A in DG SOI N-MOSFET at V_{GS} = 0V and V_{DS} =3.3V (Fig. 9 and Fig. 10).

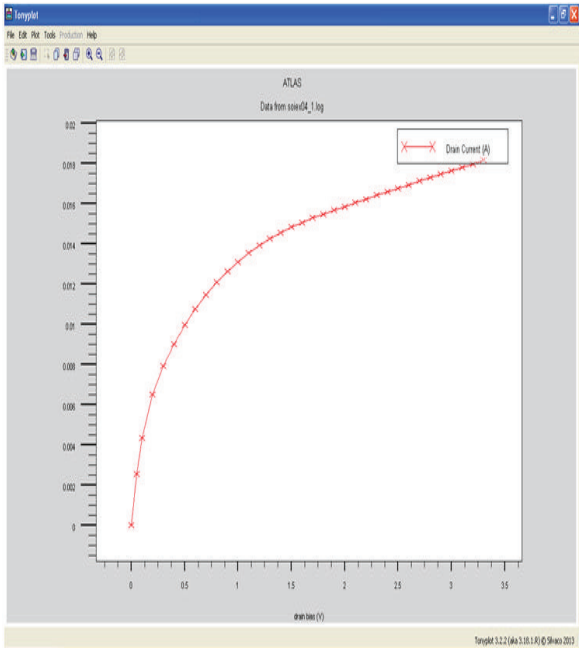

Figure 9. The leakage current output of SOI N-MOSFET.

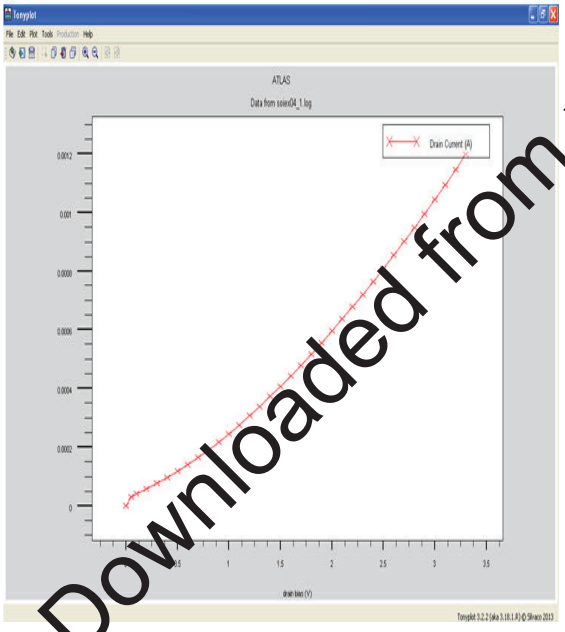

Figure 10. The leakage current output of DG SOI N-MOSFET.

From Fig. 11 and Fig. 12, it is observed that subthreshold slope of 0.292386 V/decade is in SOI N-MOSFET and 0.124954 V/decade in DGSOI N-MOSFET at V_{DS}= 0.1V.

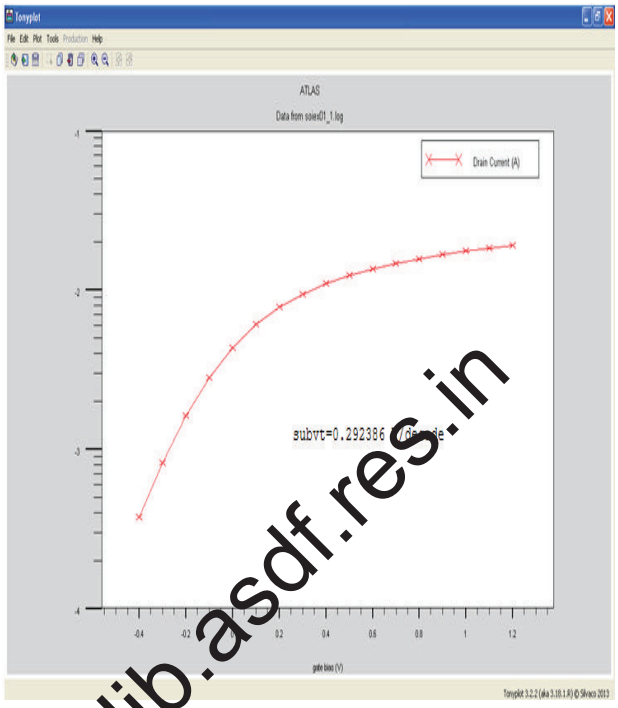

Figure 11. I_{DS}-V_{GS} subthreshold voltage of SOI N-MOSFET.

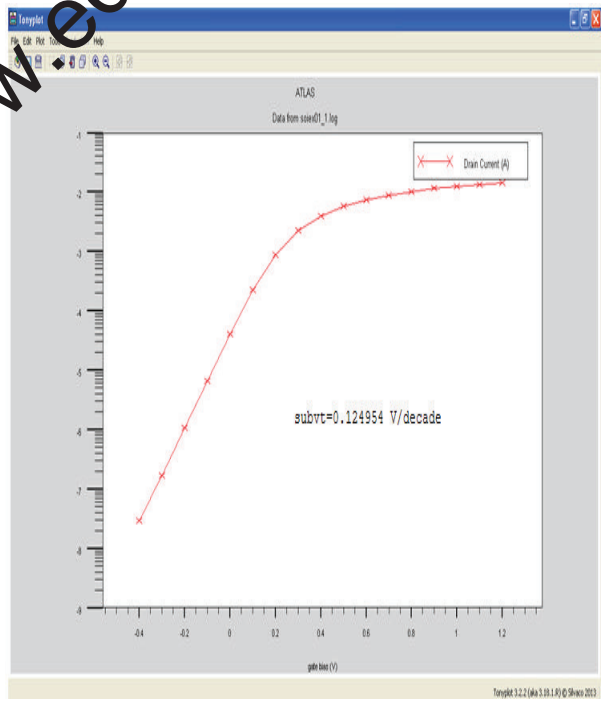

Fig. 12. I_{DS}-V_{GS} subthreshold voltage of DG SOI N-MOSFET.

VI. CONCLUSION

The comparison of electrical characteristics of single gate SOI N-MOSFET with double gate DG SOI N-MOSFET was done successfully.

The characteristics of SOI N-MOSFET and DG SOI N-MOSFET are obtained by using of numerical simulation tool Atlas.

It is concluded that of DG SOI N-MOSFET has lower leakage current than SOI N-MOSFET. The threshold voltage of DG SOI N-MOSFET is better than those corresponding to SOI N-MOSFET and the saturation current I_{DSAT} east liked significant in the DG SOI N-MOS compared to the SOI N-MOSFET transistor.

At the end of this paper, we observe that simulation results we obtained are comparable to the results encountered in theory and are thus considered very promising and satisfactory.

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