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Low Swing in Clock Pair Shaired Implicit Pulsed Flip-Flop

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Abstract— *Power consumption is a major bottleneck of system performance a large portion of the on chip power is consumed by the clock system which is made of the clock distribution network and flop-flops. An effective way to reduce capacity of the clock load by minimizing number of clocked transistors .The proposed low-swing in clock pair shared implicit pulsed flip-flop (LS-CPSIPFF) operates with a low-swing sinusoidal clock through the utilization of reduced swing inverters at the clock port. The LS-CPSIPFF enables 6.5% reduction in power compared to the full swing flip-flop with 19% area overhead. The LS-DCCFF has 870 ps longer data to output delay as compared to the full-swing flip-flop at the same setup time for a 100 MHz sinusoidal clock.*

Index Terms—*Delay, flip-flop, low-swing, power, resonant clocking, low-swing in clock pair shared implicit pulsed flip-flop (LS-CPSIPFF)*

I. INTRODUCTION

Due to the increasing demand on portable applications and the increased cost of cooling, low-power has become a crucial design objective. Resonant clocking has demonstrated significant advantages in terms of power savings compared to conventional square-wave clocking resonant clock generators with programmable driver and reference pulses, none of them have addressed the need to estimate the required driver strength at an early stage of the design. Estimation the required driving capability of the driver in the resonant clock generator [1].

The system on chip (SoC) design is integrating hundreds of millions of transistors on one chip, whereas packaging and cooling only have a limited ability to remove the excess heat. All of these results in power consumption being the bottleneck in achieving high performance and it is listed as one of the top three challenges in ITRS 2008. The clock system, which consists of the clock distribution network and sequential elements (flip-flops and latches), is one of the most power consuming components in a VLSI system [1], [2]. It accounts for 30% to 60% of the total power dissipation in a system [1]. As a result, reducing the power consumed by flip-flops will have a deep impact on the total power consumed.

A large portion of the on chip power is consumed by the clock drivers. Caution must be paid to reduce clock load when designing a clocking system. Resonant clocking enables the generation of clock signals with reduced power consumption. The traditional approach for LC resonant CDNs is to use the LC tank to drive the global clock distribution while the local square clock is being delivered through conventional buffers. However, around 66% of clock power is being dissipated in the last buffer stage driving the flip-flops [4], leading to minor power savings in LC globally-resonant locally-square CDNs. In order to achieve maximum power savings, the LC tank should drive the entire clock network (both global and local) without using intermediate buffers. This would require designing, modifying and understanding flip-flop performance with the sinusoidal clock signal generated in LC resonant networks.

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In this paper, we introduce a low-swing differential conditional capturing flip-flop (LS-DCCFF) for use in low-swing LC resonant CDNs. As far as the authors know, this is the first application of low-swing clocking to LC resonant CDNs. In our approach, no additional power supply is required to achieve low-swing clocking. We have characterized a frequency dependent delay associated with driving the pulsed flip-flop with a low-swing sinusoidal clock.

Power consumption is determined by several factors including frequency f, supply voltage v, data activity, capacitance c, leakage, and short circuit current. [3]

$$P = P_{dynamic} + P_{short\text{-}circuit} + P_{leakage} \quad (1.1)$$

In the above equation, dynamic power $P_{dynamic}$ is also called the switching power,

$$p_{dynamic} = c.VDD.VP.f \quad (1.2)$$

In the above equation c denotes the output capacitance, vdd is the supply voltage, vp is the peak voltage stored on that capacitor and f denotes the frequency.

$P_{short\text{-}circuit}$ is the short circuit power which is caused by the finite rise and fall time of input signals, resulting in both the pull up network and pull down network to be ON for a short while

$$P_{shortcircuit} = I_{shortcircuit}. VDD \quad (1.3)$$

$P_{leakage}$ is the leakage power. When the supply voltage scaling down, the threshold voltage also decreases to maintain performance. However, this leads to the exponential growth of the sub threshold leakage current. Sub threshold leakage is the dominant leakage now.

$$P_{leakage} = I_{leakage} VDD \quad (1.4)$$

Based on these factors, there are various ways to lower the power Consumption. They are 1) Double Edge Triggering 2) low swing voltage 3) switching activity 4) Reducing short circuit power 5) Reducing leakage power 6) Reducing capacity of clock load [5]. In this paper we proposed first two techniques to reduce the amount of power consumption in differential conditional capturing flip-flop. To execute low swing voltage we proposed low swing inverters by which the peak voltage of input sinusoidal waveform is reduced to (Vdd-Vtp).

The remainder of this paper is organized as follows. A description of the proposed LS-DCCFF and a characterization of the delay associated with LC low-swing clocking are presented in Section II. Section III describes the test chip. Section IV includes simulation and measurement results obtained. The conclusion of this paper is provided in Section V.

II. Low-Swing LC Resonant Clocking

A) LS-CPSIPFF

Fig. 2.1 shows the proposed LS-DCCFF. Conditional capturing flip-flop is used to avoid unwanted internal switching activity in the internal nodes of the flip-flop. As shown in Fig. 2.1, reduced swing inverters similar are used at the node fed by the low-swing sinusoidal clock signal. This is done to reduce the short circuit power. To operate the MOSFET in saturation region drain to source voltage (v_{ds}) should be greater than difference of gate to source voltage and threshold voltage.

$$V_{ds} > V_{gs}\text{-}V_t \text{ (in saturation)} \quad (2.1)$$

The load pmos transistor in the reduced swing inverters is always in saturation since $V_{gs} = V_{ds}$. It lowers the voltage at the source of the second pMOS in each inverter to approximately VDD-V_{tp} [7]. The peak voltage for the low swing clock was chosen to be equal to 0.65V since VDD =1V and threshold voltage of pMOS transistor is approximately -0.34V.

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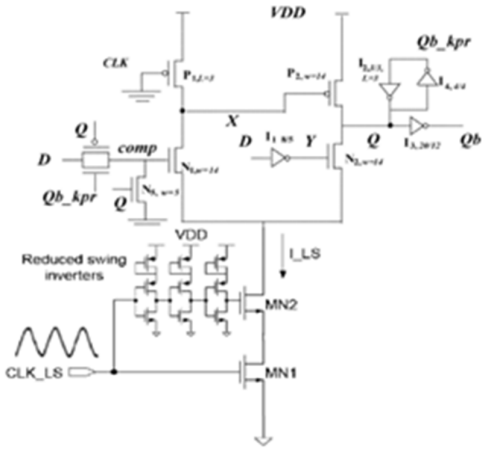

Fig 2.1 LSCPSIPFF

B. Delay Associated with Low swing LC Resonant Clocking

Resonant clock signal is applied to transistor MN1 and low swing sinusoidal clock signal is applied to MN2. $V_{pulldown}$ is the voltage level at which transistors MN1 and MN2 turned on by which pull down node SET/RESET to lower voltage level required to trigger the NAND latch. From Fig.2.2 we can able to see that there is a time difference between full swing and low swing sinusoidal clock to reach $V_{pulldown}$. Thus low swing sinusoidal clock experiences longer data as compared to full swing.

In the following, an analysis is conducted to estimate the delay in reaching $V_{pulldown}$ for low swing resonant clock signal. Let the full- and low-swing clock signals be given by the following equations:

$$V(t)_{fullswing} = 1/2\ VDD\ \sin[70]\ [(2\pi fT-\pi/2)+1/2\ VDD] \quad (2.2)$$

$$V(t)_{lowswing} = 0.65/2\ VDD\sin(2\pi fT-\pi/2)+1/2\ VDD \quad (2.3)$$

where f is the clock frequency, VDD and 0.65VDD are the peak voltage for full-swing and low swing sinusoidal clock signals respectively. Referring to Fig 2.2 and substituting the value

$$V_{pulldown}=1/2\ VDD\sin(2\pi fT1-\pi/2)+1/2\ VDD \quad (2.4)$$

From which

$$T1= 1/2\pi f(\sin-1((2\ Vpulldown)/VDD-1)+\pi/2\ ) \quad (2.5)$$

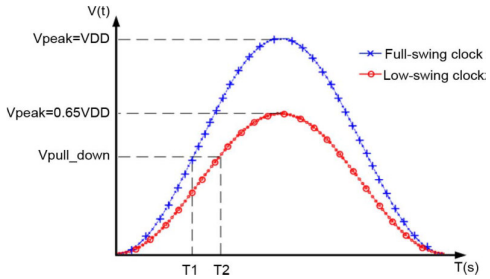

Fig.2.2. Delay between the low and full-swing resonant clock signals to reach Vpull-down

Using the same approach for low swing clock signal

$$T2 =1/2\pi f\ (\sin-1((2\ V_{pulldown})/0.65VDD-1)+\pi/2) \quad (2.6)$$

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The time difference between two clock signal to reach $V_{pulldown}$ between low and full-swing flip-flops is given by,

$$T2-T1=1/2\pi f\ (\sin^{-1}(2Vpulldown/0.65VDD-1)-\sin^{-1}(2Vpulldown/VDD-1)) \quad (2.7)$$

The above equation gives the delay between the full and low swing flip-flops. It illustrates that this delay is inversely proportional to clock frequency i.e at higher frequencies, the delay decreases.

C) Power

The power dissipation of the resonant clock network is given by following equation:

$$P_{resonant\_clock}=Rclk/2(\pi fVpeak(Cclk+\alpha NCFF))2 \quad (2.8)$$

Where R_{clk} and C_{clk} are the clock capacitance and resistance as seen by the driver, f and Vpeak are the frequency and peak voltage of generated clock signal ,CFF is the loading capacitance of the flip-flop, N is the number of flip-flops and α is the factor by which the loading capacitance of the flip-flop connected at the clock leaves is reflected to the driver side . The above equation illustrates that generating a low swing clock signal with V_{peak} = 0.65 VDD results in around 58% power reduction in clock network.

IV. Performance Analysis

The LS-DCCFF enables 6.5% reduction in power compared to the full-swing flip-flop due to low swing by which peak voltage of input sinusoidal wave is reduced to 0.65VDD and also it results in 58% power reduction in clock network. The output of full swing clock and low swing clock is shown in Fig.3.1.

In Fig 3.1 red color swing represent the full swing whereas green color swing represent the low swing resonant clock signals. It is clear that low swing resonant clock signal reduces the peak voltage of input signal and thereby reducing the power consumption in DCCFF.

The original input data (D) and full swing input is shown in Fig3.2. The delay associated with full-swing and low swing LC resonant clocking scheme output is shown in Fig, 3.3

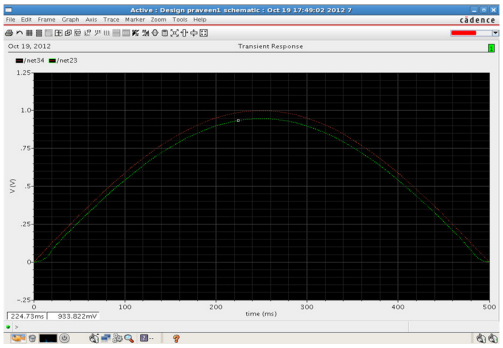


Fig 3,1. Low-swing (green) and full-swing (Red) resonant clock signal

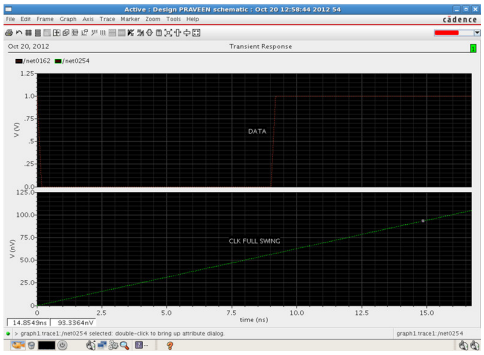


Fig 3.2 Original input data(D) and full swing input.

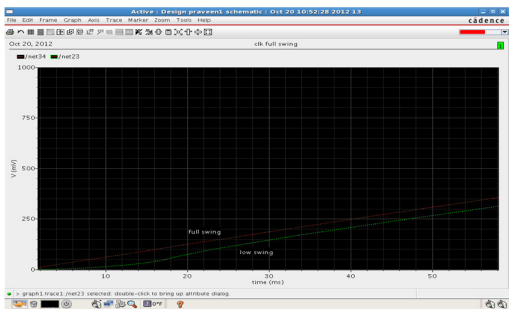
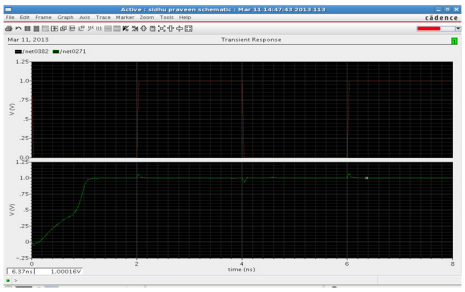


Fig 3.3 Delay associated with full-swing and low swingFig



3.4 Input of D and Output of Q in CPSIPFF

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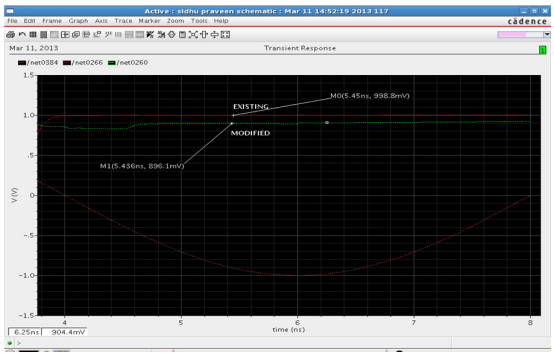

Fig 3.5 output of CPSIPFF existing and modified

Table I: Area and power comparison between full- and low-swing clocking

Contents	LSCPSIPFF
Area (μm^2)	43
% increase in area compared to full swing	19
Power (μW)	4.58
% decrease in power compared to full swing	17.5

V. Conclusion

We have proposed a low-swing sinusoidally clocked flip-flop to obtain further power reduction in LC resonant CDNs. Low-swing resonant clocking in pulsed flip-flops results in a delayed flip-flop response. Theoretical analysis has been performed and the delay associated with low-swing sinusoidal clocking was characterized.

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