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Implementation of Low Power Viterbi Decoder Using FPGA

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Abstract: *In Communication Engineering, Convolutional encoding is a forward correction technique which is used for error correction at the receiver. Viterbi algorithm is used for decoding the Convolutional encodes and one of the best techniques for decoding. The basic building blocks used for Viterbi decoder are branch metric unit; add compare select unit and survivor memory unit. The 'Trace back' is used to decoding the data. Though 'Trace back method has larger decoding time, it is used for longer constraint length.*

In this paper, Viterbi decoder with 'trace back' method is used and the decoder is designed with a constraint length of 7 and code rate of 1/3 for an efficient purpose. The Viterbi decoder has an efficient memory organization, low hardware complexity and lower power dissipation. The design is synthesized using Xilinx 14.1 software and the implementation is done using FPGA-Spartan 3E.

Keywords: *Viterbi decoder, Convolutional encoder, Branch metric unit, Path metric unit, survivor unit, FPGA-Spartan, verilog module.*

INTRODUCTION

For communication system, the error detection, and correction are important for reliable communication. But error detection techniques have some disadvantages. It reduces the throughput continuously. To compensate the White Gaussian noise, error correction technique is used. Forward error correction improves throughput.[1] The aim of VLSI is to reduce area; and power to achieve high speed.[2] The low power should be demoralized for the Viterbi decoder to reduce complexity as well as power utilization. The advantage of viterbi decoder is fixed decoding time, for hardware decoder [3]. The viterbi algorithm performs maximum likelihood decoding and it corrects the errors in the received data which is caused by the channel noise. Viterbi decoder requires a processor which implements the viterbi algorithm depending on the uses of application [4]. SMU (survivor memory unit) decisions are stored in the ACS (add-compare select) unit and used to compute the decoding output. SMU is designed by serial-in-serial-out shift register and these register length depending on Convolutional encoder [5]. FPGA (Field programmable gate array) has programmable logic components and interconnects. It used the memory which is static and reprogrammable [6].Spartan-3E is used for applications of electronics and broadband access.

Literature Review

V.Prasanth proposed a scheme based on verilog language for "Implementation of speed and power optimization of FPGA using a viterbi decoder". Trellis coded modulation is proposed. In this viterbi algorithm priority encoder is used with Convolutional encoder to send the data bits. This reduces the power consumption of 80% without loss. This architecture which uses clock speed is negligible. Proposed architecture is synthesized using FPGA-Spartan 6.

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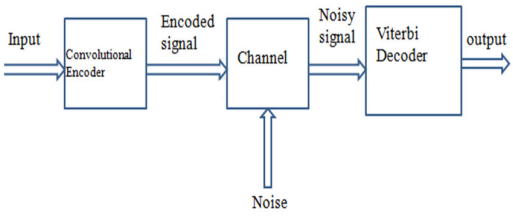
Saradha Suresh Dambal presented a "Design and simulation of hybrid modified viterbi decoder for fast communication". For communication purpose VLSI recommends less power, area and also delay. In this unit hybrid is placed between ACS and SMU. And this hybrid unit reduces the memory blocks. This unit uses two clock cycles, one for trace back information and another for storing the information in register block. The simulation has an operating frequency of Convolutional encoder is 74.91 MHz.

Sherif Welsen Seker discussed "Implementation of Low power viterbi decoder for software–defined WiMAX receiver". In wireless communication viterbi algorithm is used to decode the Convolutional codes along with this is used in digital communication system. In signal processing FPGA is considered as highly configurable. In this architecture viterbi decoder for WiMAX receiver is used along with VHDL code. The design is implemented on Xilinx virtex.

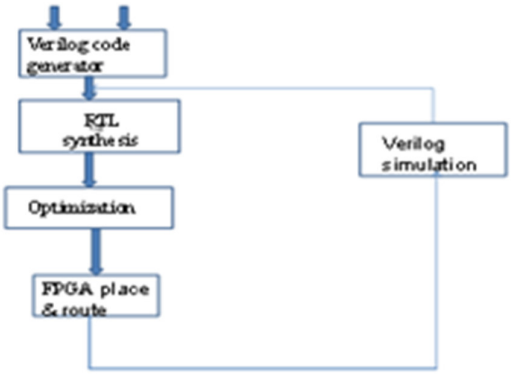
K.Rajendar presented a paper on "FPGA Implementation of efficient Viterbi decoder for Multi-carries systems". In this adaptive viterbi decoder which are used in digital communication system. An alternative approach is provided to the block codes for transmission over noisy channel. The Convolutional coding is applied to both data stream and data blocks. For fast decoding process a method called "PNPH"(permutation Network based path History).It uses the constraint length ,of 3(k) and code rate of ½(k/n)by verilog module. In this simulation is done on Xilinx virtex.

Process of Viterbi Decoder



Information is transmitted to the convolutional encoder, where the errors are corrected by a mechanism called error correcting code. The convolutional encoder has n-modulo 2 adders and n- generator polynomials for each adder. For Convolutionally encoded data the memory register starts holding with 1 input bit unless memory registers start with 0.the viterbi algorithm 'asymptotically optimum' approach, It is also known as maximum likelihood decoding algorithm for convolutional algorithm. This decoding algorithm is used for finding the code branch in code trellis, which is most likely transmitted. By reducing the complexity the viterbi algorithm performs ML decoding.

In viterbi decoder three basic units are used such as Branch metric unit, Path metric unit and Survivour memory management unit with Trace back method.



Methodology

Initially for the hardware design an intermediate representation is produced. The production of intermediate representation is synthesis and the result is a netlist which is device independent. In the above step the errors and detailed description of errors are created and verified. Netlist is usually stored in the standard format called Electronic Design Interchange Format (EDIF).

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In simulation a software program known as simulator is used to verify the functionality of the circuit. The code's functionality is verified and corresponding output is checked. If the output verified is correct simulation converts the output waveform into zeros and ones.

Conclusion

For decoding the Convolutional codes a most suitable technique known as viterbi decoding is used. In viterbi coding a constraint length of 7, code rate of 1/3 is developed. Using Trace back method the energy consumption is reduced. Trace back method is one of the decoding techniques for decoding Convolutional codes. Since ACS unit consumes more power, a Bit serial approach is implemented in order to reduce the amount of interconnections in bit serial architecture which in turn reduces the energy consumption further.

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