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Design and Implementation of Low Power FIR Filter using Integrated Multiplier

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Abstract – *In this research work, design and analysis of Finite-Impulse Response (FIR) Filter using different multipliers with an algorithm namely called Common Subexpression Elimination (CSE) is presented. The Booth and array multiplier reduces the switching activity but consumes more power. Hence the hybrid encoded low power multiplier consumes less power. Based on the number of one's present in the multiplier, hybrid encoded low power multiplier works. CSE algorithm is a technique where fixed coefficient multipliers are replaced with a series of add and shift operations implemented using hybrid encoded low power multiplier. A modified CSE algorithm reduces the number of adders while maintaining performance in hybrid encoded low power multiplier can achieve power savings ranging from 10% to 12% compared to other multipliers at the expense of minor control degradation.*

Index Terms— *Finite-Impulse Response (FIR), Common Subexpression Elimination (CSE), Array multiplier, Booth multiplier, Hybrid encoded low power multiplier.*

I. INTRODUCTION

FIR digital filter is widely used as a basic tool in various signal processing and image processing applications. Signal Processing is used everywhere to extract information from signals or to convert information carrying signals from one form to another it means operation that changes the characteristics of a signal. Processing of such signals includes storage and reconstruction, separation of information from noise (e.g., aircraft identification by radar), compression (e.g., image compression), and feature extraction (e.g., speech-to-text conversion). These characteristics include the amplitude, shape, phase and frequency content of the signal. The order of an FIR filter primarily determines the width of the transition-band, such that the higher the filter order, the sharper is the transition between a pass-band and adjacent stop band. Jeong-Ho Han etal has proposed to reduce the hardware complexity of FIR digital filters, this paper proposes a new filter synthesis algorithm. Also the proposed algorithm selects an adder graph that can be maximally sharable with the remaining coefficients. Ya Jun Yu etal has proposed a novel optimization technique is proposed to optimize filter coefficients of linear phase FIR filter to share common sub expressions within and among coefficients. Two-stage optimization technique suffers from the problem that the search space in the second stage is limited by the finite word length or SPT coefficients obtained in the first stage optimization. Dong Shi etal has proposed an extrapolated impulse response filter with residual compensation is proposed for the design of discrete coefficient FIR filters using sub expression sharing. The proposed technique utilizes the quasi-periodic nature of the filter impulse response to approximate the filter coefficients. Fei Xu etal has proposed an algorithm, called Contention Resolution Algorithm (CRA) for weight-two sub expressions. The performance of the algorithm are analyzed and evaluated based on benchmarked finite impulse response filters and randomly generated data.

Here we proposed a modified common subexpression elimination CSE algorithm reduces the number of adders. The goal of our optimization is to reduce the area of themultiplier block by minimizing the number of adders and any additional registers required for the fastest implementation of the FIR filter.

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The rest of this letter is organized as follows. The FIR filter is presented in Section II. The CSE ALGORITHM is presented in the section III and proposed method is explained in section in IV. The Array multiplier is described in Section V. The Booth multiplier is presented in Section VI and the context for hybrid encoded low power multiplier is described in Section VII. The experimental results are given in Section VIII. Finally, Section IX concludes this letter.

II. FIR Filter

FIR digital filters are widely employed in digital signal processing due to their stability and linear-phase property. In many applications requiring high-speed processing and low power consumption, FIR filters are implemented as dedicated filter blocks. FIR filters have many attractive virtues such as exact linear phase property, guaranteed stability, free of limit cycle oscillations, and low coefficient sensitivity. Equation (1) describes an output of L tap FIR filter, which is the convolution of the latest L input samples. L is the number of coefficients of the filter impulse response h[k], and x[n] represents the input time series. Fig 1 shows the general structure of the FIR filter.

$$y[n] = \sum_{k=0}^{N-1} h[k].x[n-k] \text{ ---------> (1)}$$

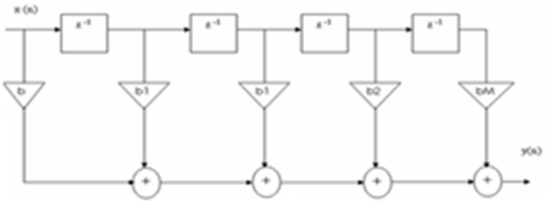

Fig 1 : General structure of the FIR filter

III. CSE Algorithm

Modified CSE algorithm to reduce area: The divisors are generated for a set of expressions and the one with the greatest value is extracted. Then the common subexpressions can be extracted and a new list of terms is generated. The iterative algorithm continues with generating new divisors from the new terms, and add them to the dynamic list of divisors. The algorithm stops when there is no valuable divisor remaining in the set of divisors. FIR filters use constant coefficients, the full flexibility of a general purpose multiplier is not required, and the area can be reduced using techniques developed for constant multiplication.. The multiplications with the set of constants {hk} are replaced by an optimized set of additions and shift operations. Finding and factoring common subexpressions can further optimize the expressions. The performance of this filter architecture is limited by the latency of the largest adder. The Fig2 shows the Filter structure with constant coefficient multiplier block. A popular technique for implementing the transposed direct form of FIR filters is the use of a multiplier block instead of using multipliers for each constant.

I. Proposed Method

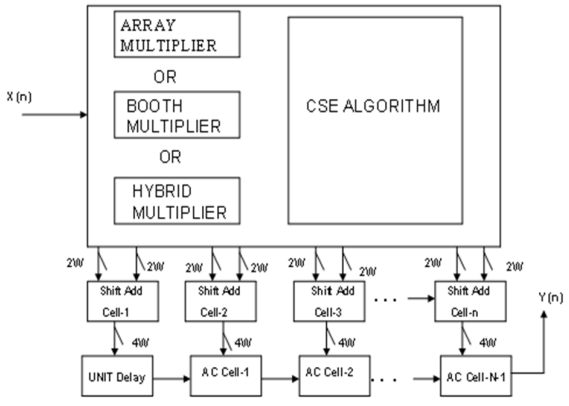

Fig 2: Block diagram of the proposed method

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The Fig 2 shows the Block diagram of the proposed method. The input signal given is defined as x(n), and the obtained output signal is defined by y(n). The CSE algorithm block acts when the same input values are used in the process. By reducing the process of executing same values the power is to be reduced.

IV. Array Multiplier

Array multiplier is an electronic hardware device used in digital electronics or a computer or other electronic device to perform rapid multiplication of two numbers in binary representation. The rules for binary multiplication can be stated as follows

- If the multiplier digit is a 1, the multiplicand is simply copied down and represents the product
- If the multiplier digit is a 0 the product is also 0 For designing a multiplier circuit we should have circuitry to provide or do the following three things:
- It should be capable identifying whether a bit is 0 or 1
- It should be capable of shifting left partial products
- It should be able to add all the partial products to give the products as sum of partial products

For Ex: A=0101 and B=0100.

```
          0101 * Multiplicand
          0100   Multiplier
-----------------------
          0000    --pp1
        0000      --pp2
      0101        --pp3
    0000          --pp4
-----------------------
 00010100         Result=20.
```

Fig 3 : Result of Array Multiplier

V. Booth Multiplier

Booth algorithm gives a procedure for multiplying binary integers in signed –2's complement representation. Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation. Booth used desk calculators that were faster at shifting than adding and created the algorithm to increase their speed. Booth's algorithm is of interest in the study of computer architecture. Booth's algorithm involves repeatedly adding one of two predetermined values multiplicand and multiplier to a product P, then performing a rightward arithmetic shift on P. The Fig 4 shows the Result Obtained in Booth Multiplier.

For Ex: A=0101 and B=0100.

```
    0101*          --Multiplicand
    01000          --Multiplier
    (1*A) (0*A)  --Booth Recoding
    ------------------------------
    00000000         --pp1
  00000101           --pp2
    ------------------------------
 0000010100       --Result=20
    ------------------------------
```

Fig 4: Result of Booth Multiplier

VI. Hybrid Multiplier

According to the conventional shift and add multiplication, the number of partial products (PP) are equal to the number of bits in the multiplier. The number of partial products can be reduced by half using Booth recoding. In the proposed encoding technique, the partial products can still be reduced which in turn reduces the switching activity and power consumption. The operation can be defined according to the number of 1's and its position in the multiplier. The Fig 5 shows the Result Obtained in Hybrid Multiplier.

For Ex: A=0101 and B=0100.

```
0101*   Multiplicand
0100    Multiplier (Category B)
-----------------
 00010100          --Result=20
-----------------
```

Fig 5: Result of Hybrid Multiplier

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VII. Results

The Table1,2,3,4,5 shows power consumption for different multipliers without the CSE algorithm for the FIR filter with various taps like 10,20,30,40,50. For all the taps the table shows the area and power of the array, booth multiplier and hybrid encoded low power multiplier. Also the fig 6,7,8 shows the power report of the array, booh, and hybrid multiplier. Power consumption is measured by using SYNOPSYS DC tool.

Array Multiplier Power Report for Tap-20 Filter

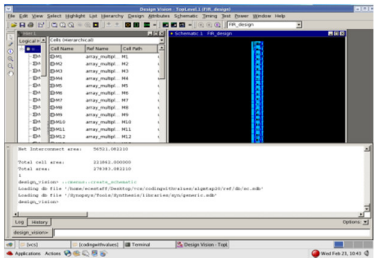

Fig 6: Array Multiplier Power report

Booth Multiplier Power Report for Tap-20 Filter

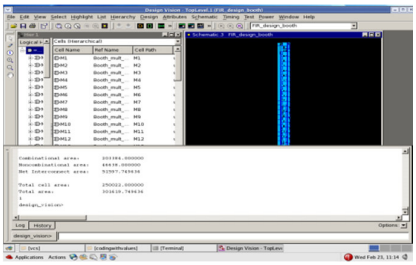

Fig 7: Booth Multiplier Power report

Hybrid Multiplier Power Report for Tap-20 Filter

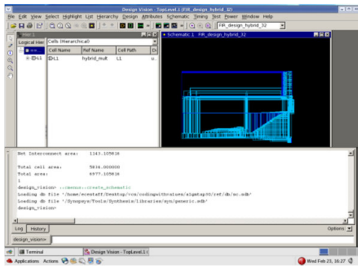

Fig 8: Hybrid Multiplier Power report

Table 1: Comparison of Area and Power for FIR filter (Tap-10) with Various Multipliers

MUTIPLIER TYPES	TAP -10	
	AREA	POWER
ARRAY MULTIPLIER	279775.8	475.2835mw
BOOTH MULTIPLIER	302730.6	408.7806 mw
HYBRID MULTIPLIER	8817.034	303.229uw

TABLE 2: Comparison of Area and Power for FIR filter (Tap-20) with Various Multipliers

MUTIPLIER TYPES	TAP- 20	
	AREA	POWER
ARRAY MULTIPLIER	278383.08	521.4363mw
BOOTH MULTIPLIER	301619.74	464.9298mw
HYBRID MULTIPLIER	8817.0340	303.22uw

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TABLE 3: Comparison of Area and Power for FIR filter (Tap-30) with Various Multipliers

MUTIPLIER TYPES	TAP-30	
	AREA	POWER
ARRAY MULTIPLIER	277024.596	567.451mw
BOOTH MULTIPLIER	300508.829	525.9819mw
HYBRID MULTIPLIER	6977.105	270.484uw

TABLE 4: Comparison of Area and Power for FIR filter (Tap-40) with Various Multipliers

MUTIPLIER TYPES	TAP-40	
	AREA	POWER
ARRAY MULTIPLIER	275700.35	613.37mw
BOOTH MULTIPLIER	299397.90	586.45mw
HYBRID MULTIPLIER	6651.62	270.46uw

TABLE 5: Comparison of Area and Power for FIR filter (Tap-50) with Various Multipliers

MUTIPLIER TYPES	TAP -50	
	AREA	POWER
ARRAY MULTIPLIER	274319.04	658.13mw
BOOTH MULTIPLIER	298286.988	647.65mw
HYBRID MULTIPLIER	5125.31	270.44uw

VIII. Conclusion

In this paper, we presented a technique based on add and shift method and common sub expression elimination for low area, low power and high speed implementations of FIR filters. The modified CSE algorithm leads to 10% to 12% power savings with little degradation in area. With the proposed architecture, larger computation power savings can be achieved at the expense of additional computation complexity.

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