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An Efficient Implementation and Analysis of Low Power High Performance Multipliers

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Abstract- Multipliers are optimized for low power which is of great interest in scientific and engineering field. There is large consumption of energy during the multiplication and addition process so an efficient implementation and analysis of different multipliers and adders are to be made to increase the performance. The multipliers used in multiplication process should involve low area, power and delay. Hence there is a need for optimization, as the performance of multiplier depends on the Multiplication process. The proposed work comprises the designing of 8-bit array multiplier and Baugh Wooley multiplier and analyzing the various parameters involved for optimizing the performance. The work has been done in a schematic editor using Tanner tool v7.00 in 20um CMOS technology. T-spice is used as simulator and W-editor is used for formal verification of the multiplier

Keywords: Array multiplier, Baugh Wooley multiplier, Area, Power, Delay.

I INTRODUCTION

Multipliers play an important role in today's digital world. Multiplication is a heavily used arithmetic operation that figures prominently in scientific applications. The motive of our project is to study and develop an Efficient Fast and Low Power Multiplier. As the name suggests we had to go for faster and low power factor optimization simultaneously. We know that the basic building block of a multiplier is ADDER circuit. The basic components used in multipliers is AND gates and few full adders. Multiplication process involves three steps:

1. Partial product generation.
2. Partial product reduction.
3. Final addition.

For the multiplication of an n -bit multiplicand with an m bit multiplier, m partial products are generated and product formed is $n + m$ bits long. Depending upon the size of the inputs multiplication operation includes the operations of shift and addition. Because of the more steps for the calculation, multiplier occupies the large area with high power consumption and low speed due to the delay. Designing of multipliers, verifying waveforms, then finally calculating area and Power consumed in the circuit. After knowing all this we also calculated delay for different multipliers which helped us to determine the best multiplier.

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II Multipliers

A. Array Multipliers

Array multiplier is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product is shifted according to their bit orders and then added. The addition can be performed with normal carry propagate adder. $N-1$ adders are required where N is the multiplier length.

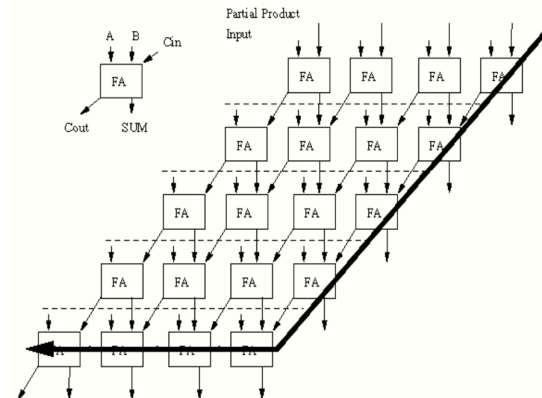


Figure 1. Array Multiplier

In Array multiplier, almost identical cells array is used for generation of the bit-products and accumulation. All bit-products are generated in parallel and collected through an array of full adders or any other type of adders and final adder. Therefore, among other multiplier structures, array multiplier takes up the least amount of area.

B. Baugh-Wooley

Baugh-Wooley algorithm for the unsigned binary multiplication is based on the concept shown in figure. The algorithm specifies that all possible AND terms are created first, and then sent through an array of half-adders and full adders with the Carry-outs chained to the next most significant bit at each level of addition. Negative operands may be multiplied using a Baugh-Wooley multiplier. A single full adder circuit naturally lays out in a very wide (or tall) chip, which creates problems when working toward smallest form factor and efficiency of cost.

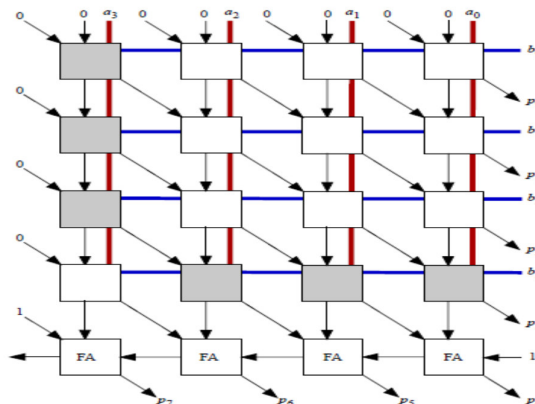


Figure 2. Baugh Wooley Multiplier

III Result

The circuits are designed and simulated using TANNER software. The implementation of the multipliers in Tanner is used to easily understand the different designing parameters effectively. The multiplier with low power eliminates the switching activities and thus

reduces the power dissipation. The 8-bit Array and Baugh wooley multiplier have been implemented. The schematic and the simulation result for the 8-bit array multiplier is shown in the Figure 3 and Figure 4.

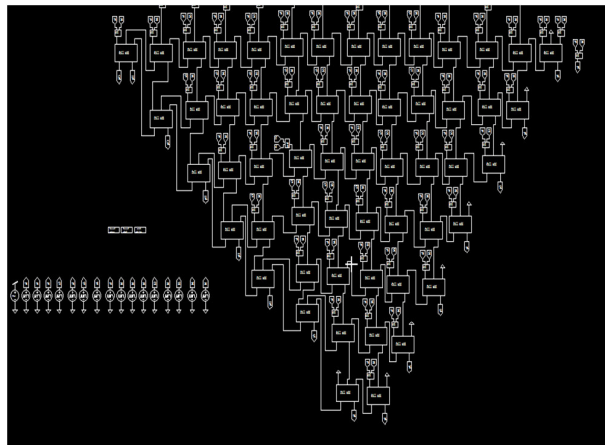


Figure 3 Schematic diagram of 8-bit Array Multiplier

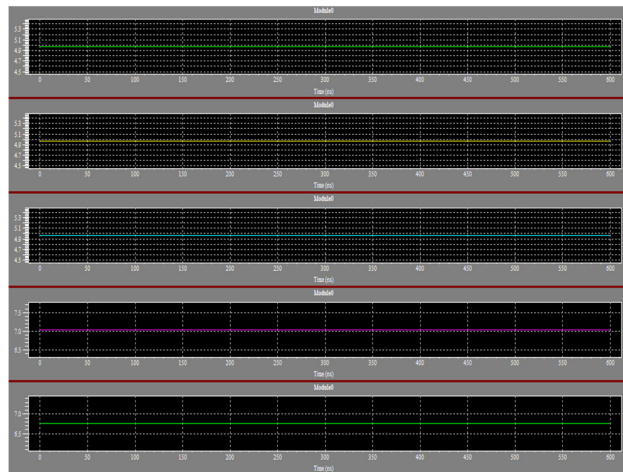


Figure 4 Simulation result of 8-bit Array Multiplier.

The schematic and the simulation result for the 8-bit Baugh Wooley multiplier is as shown.

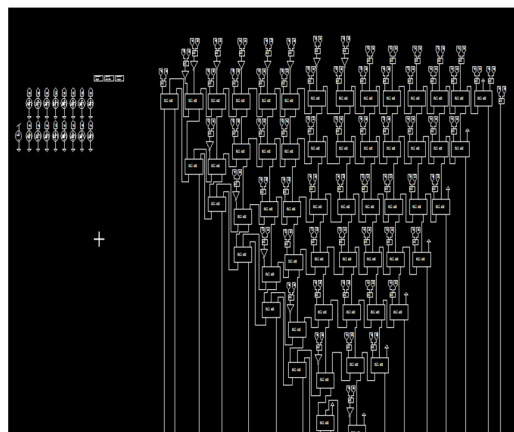


Figure 5 Schematic diagram of 8-bit Baugh Wooley Multiplier

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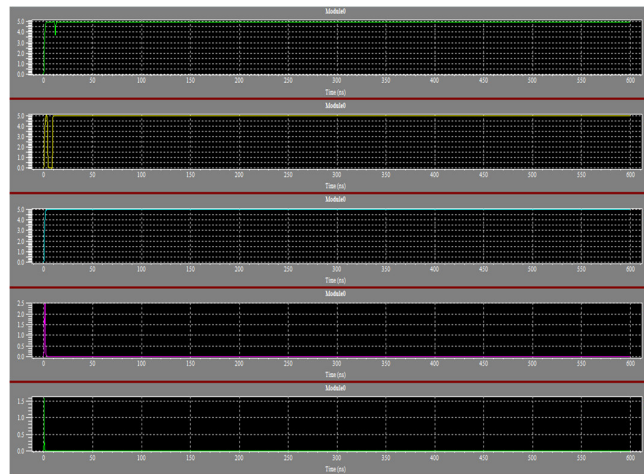


Figure 6 Simulation result of 8-bit Baugh Wooley Multiplier

Table I shows the comparison of Array multiplier and Baugh Wooley multiplier. The comparison is done on the basis of Power, Area and Delay. Array multipliers possess the best features compared to Baugh Wooley multiplier. Array multiplier has the low delay of 16.91ns. So the array multiplier has the highest speed when compared to the Baugh Wooley multipliers. Enhancement of speed always results in large area. Hence we should use Array multiplier when it comes to optimization with both Area and Time. It can be concluded that Array Multiplier is superior in all respect like speed, delay, area, Regular structure, power consumption.

Table I Comparison of Multiplier

	Power	Area	Delay	PDP
Array Multiplier	3.463151e-002	3904 um	16.91 nsec	58.561 wsec
Baugh Wooley Multiplier	3.610487e-002	3960 um	24.82 nsec	89.61 wsec

IV Conclusion

After going through all the hard work and facing problems, this project managed to complete its objectives that are to implement different Multipliers and learn the Power and Time trade off among them so that we can design Efficient Faster Low Power Multiplier as Low power consumption is the most important criteria for the high performance. It can be concluded that Array Multiplier is superior in all respect like speed, delay, area, Regular structure, power consumption compared to Baugh Wooley multiplier.

V Future Scope

As an attempt to develop multiplier algorithm and architecture level optimization techniques for low-power multiplier design, the research presented in this dissertation has achieved good results and demonstrated the efficiency of high level optimization techniques. However, there are limitations in our work and several future research directions are possible with many other multipliers.

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