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An adjustable Comparator for 2-bit/step SAR ADC Configuring with multiple samples per second in 40nm CMOS

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Abstract: *A low-power 2-bit/step operation technique is proposed which uses dynamic threshold configuring comparator instead of multiple digital-to-analog converters (DACs). Power and area overhead is minimized by successively activated comparators. The comparator threshold is configured by simple Vcm biased current source, which keep the ADC free from power supply variations over 10%. To implement power efficient and high performance analog-to-digital converters the designers are urged to design an optimized dual tail comparator. In this paper, It is shown that in the proposed dual tail comparator both the power and delay time is significantly reduced.*

Keywords: *Successive Approximation Register (SAR), high speed analog to digital converter (ADC), Dynamic threshold comparator, Dual tail comparator.*

I. INTRODUCTION

To Provide ubiquitous computing, demand for low power circuits is expanding. Handheld mobile devices such as smartphones communicate with a server to provide various functions. However, in the future, smartphones will also connect to other hardware devices, such as medical devices and sensor nodes, as well [1]. Such ubiquitous computing will create more innovative applications but there are severe challenges in hardware design. As the wireless trafficis predicted to increase massively, the power consumption of wireless circuits is to increase simultaneously as well, far beyond the growth of battery capacity. Therefore, we focus on designing low-powered analog-to-digital converters (ADCs)

Many low-power ADCs for radios and sensor nodes has been proposed, most using the successive-approximation register (SAR) ADC architecture [2]–[4]. This architecture has a superior power efficiency compared with the other architectures which use power-hungry op-amps. A number of highly power efficient designs has been presented at low-speed domains. By improving the charge-redistribution digital-to-analog converters (DACs) [2] and using 500 Af unit capacitors in the DAC [3], analog power consumption was reduced significantly. SAR ADC can achieve high power efficiency at a high resolution by designing reconfigurable comparators [4] and majority voting [5].Although in most of the research, the operating speed is within sensor application and insufficient for radio requirements which often demand ADCs operating over few tens of MS/s. The SAR ADC has a bottleneck of speed, because the SAR search algorithm requires n clock cycles to obtain an n bit resolution. We have worked on improving the speed of lowpower SAR ADCs in the past, by optimizing the delay time of each cycle. However, the speed increased by only 20% [6]. Considering that SAR ADC consumes only dynamic power, time interleaving will be a good way to provide high-speed operation [7].In this paper, a comprehensive analysis about the delay of dynamic comparators has been presented for various architec-tures. Furthermore, based on the dual tail structure proposed in [10], a new dynamic comparator is presented, which does not require boosted voltage or stacking of

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too many transistors. Merely by adding a few minimum-size transistors to the conventional dual tail dynamic comparator, latch delay time is profoundly reduced. This modification also results in con-siderable power savings when compared to the conventional dynamic comparator and dual tail comparator.

II. Architecture Model

A. 2-bit/Step WithDynamic Threshold Comparators

2-bit/step ADC with successively activated comparators (SAC) and the block diagram and operation concept is shown in Fig. 2. After the external sampling clock (CLK ext) sets down, an SA cycle 1starts by rising φ1 and CP1 decides the first bit (OUTCP1).After the first bit decision, VTH comp of CP2 (VTHCP2) isset and reflects the result of OUTCP1. In this case OUTCP1is 1, thus VTHCP2 is set to 12/16 V ref and the second bit (OUTCP2) is decided. In the proposed ADC, the 2-bit quantizer operates like a binary-search ADC [8], where the second comparator is activated reflecting the preceding comparator's results.

Because the second comparator threshold is configured dynamically every cycle, only two comparators are required instead of three. The register units (Cyc. N reg.) and a synchronous internal clock generator (Clock gen.) are custom designed dynamic logic cells and specific details are discussed in [9]. The results of SA cycle 1 are stored in MSB and 2ndMSB registers, respectively.

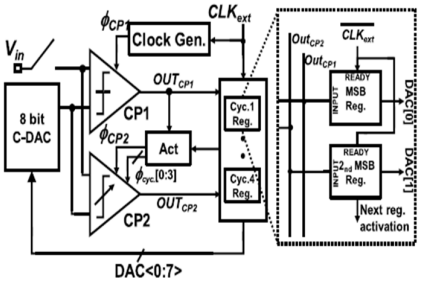
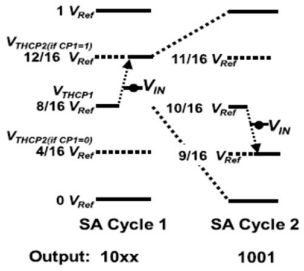


Fig. 1. Proposed 2-bit/step SAR ADC with successively activated comparators Block diagram.

Fig. 2. Operation of dynamic threshold comparator in SAR ADC



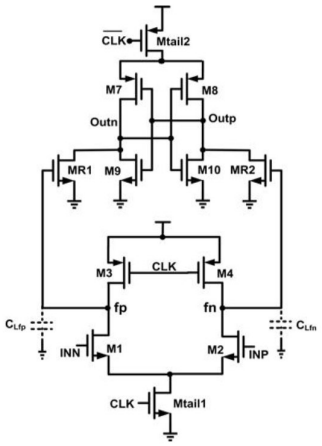


Fig. 3. Schematic diagram of the conventional dual tail dynamic comparator

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B. Conventional Dual tail Dynamic Comparator

A conventional dual tail comparator is shown in Fig. 3 [10]. Which has comparatively less power consumption. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider Mtail2, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small Mtail1), for low offset [10]. The operation of this comparator is as follows (see Fig. 4).

During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and volt-ages at nodes fn and fp start to drop with the rate defined by IMtail1/Cfn(p) and on top of this, an input-dependent differential voltage _Vfn(p) will build up.

The intermediate stage formed by MR1 and MR2 passes Vfn (p) to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of kick back noise [10].

III. Proposed Dual Tail Dynamic Comparator

Fig. 5 demonstrates the schematic diagram of the proposed dynamic dual tail comparator. Due to the betterperformance of dual tail architecture in low-voltage applications, the proposed comparator is designed based on the dualtail structure.

The mainidea of the proposed comparator is to increase _Vfn/fp in order to increase the latch regeneration speed. For this purpose, two control transistors (Mc1 and Mc2) have been added to the first stage in parallel to M3/M4 transistors but in a cross-coupled manner [Fig. 3].

A. Operation of the Proposed Comparator

The operation of the proposed comparator is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground.

During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages.

Suppose VINP > VINN, thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely.

In other words, unlike conventional dual tail dynamic comparator, in which _Vfn/fpis just a function of input transistor trans conductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp (_Vfn/ fp) increases in an exponential manner, leading to the reduction of latch regeneration time.

Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption.

IV. Simulation Results

In order to compare the proposed comparator with the conventional and double-tail dynamic comparators, all cir-cuitshave been simulated.

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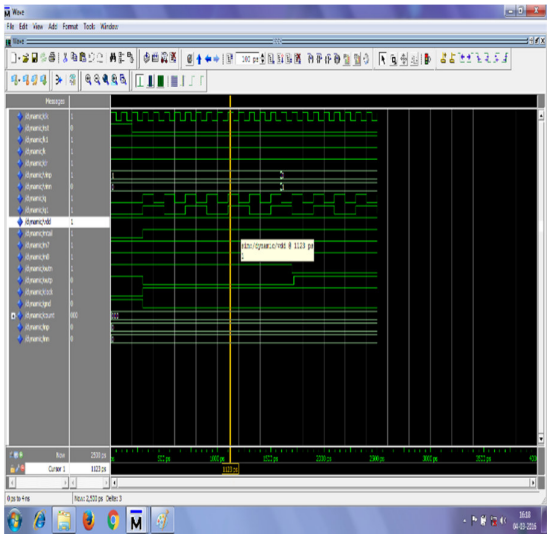

Fig.4. Simulation result of dynamic threshold comparator

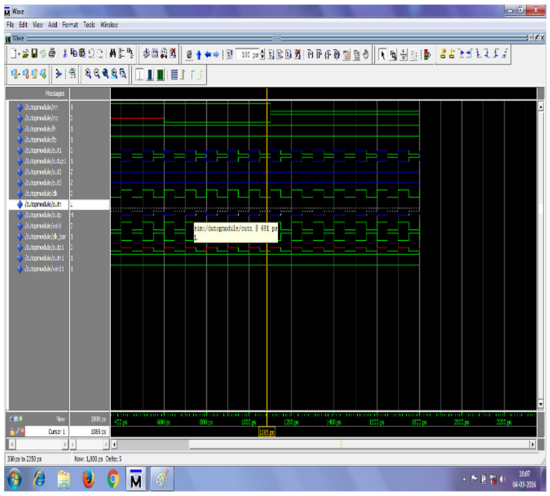

Fig.5. Simulation result of proposed dynamic dual tail comparator

Fig. 5 demonstrates the schematic diagram of the proposed dynamic dual tail comparator which is applied in SAR ADC to the application of phase generator.

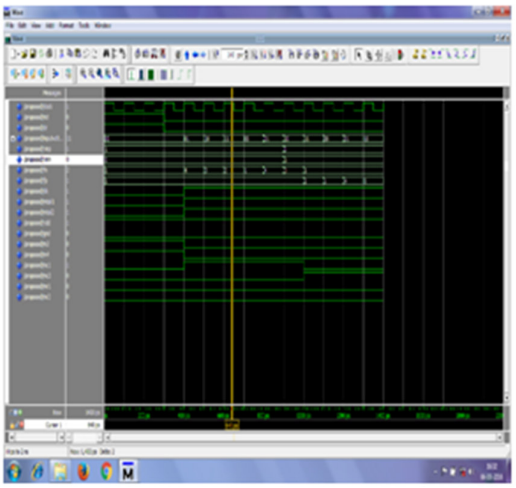

Fig.6 Simulation result of proposed comparator with SARADC

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From the figure.6, the proposed method of comparator (dual tail comparator) which has applied to the SAR ADC can be clear with power consumption and time delay.

Conclusion

In this paper, we presented a analysis of dual tail comparator in SAR ADC in terms of power, area and delay. Both comparators namely conventional threshold dynamic comparator and conventional dual tail dynamic comparators were analyzed. By Compared with conventional threshold configuring techniques, the proposed method can generate large comparator offset with small power.

The design method of the variable current source was presented and the power supply noise immunity was studied. The effect was confirmed by measurement and ADC had immunity against power supply variation of over 10%. Therefore this method can applied to the various applications of SAR ADC in which have already applied in Phase generator. With the proposed techniques, the ADC achieved over 50% speed improvement and achieved power efficiency competing with the state-of-the-art works.

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