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DESIGN OF LOW POWER-DELAY PRODUCT CARRY LOOK AHEAD ADDER USING MANCHESTER CARRY CHAIN

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ABSTRACT: *An 8-bit Manchester carry chain (MCC) adder in multi output domino CMOS logic is designed using 180nm technology. The carries of this adder are computed in parallel by two independent 4-bit carry chains. Due to its limited carry chain length, the use of the proposed 8-bit adder module for the implementation of wider adders leads to significant operating speed improvement compared to the corresponding adders based on the standard 4-bit MCC adder module. The Power-Delay Product (PDP) of proposed adder also reduced compared to the conventional adders.*

Keywords: MCC Adders, Domino logic, PDP.

I. INTRODUCTION

Addition is a fundamental arithmetic operation that is widely used in many VLSI systems and architectures, such as application specific digital signal processing (DSP) architectures and microprocessors. As the need of higher performance, there is a continuing need to improve the performance of arithmetic logic units and to increase their performance. The combination of arithmetic units and higher performance processors are used in implementing High-speed adder architectures like carry look-ahead (CLA) adders, carry-skip adders, carry-select adders, conditional sum adders [2]-[5]. High-speed adders based on the CLA principle remain dominant, since the carry delay can be improved by calculating each stage in parallel. The CLA algorithm was first introduced in [6], and several parameters have developed.

Energy efficiency is one of the most required features for designing such adders for high performance applications. The Manchester carry chain is a variation of the CLA adder that uses shared logic to lower the transistor count. It is the most common dynamic (domino) CLA adder architecture with a regular, fast, and simple structure adequate for implementation in VLSI [7]. The recursive properties of the carries in MCC have enabled the development of multioutput domino gates, which produces area-speed improvements with respect to single-output gates. In this paper, a new 8-bit carry chain adder block in multioutput domino CMOS logic is designed proposed. The even and odd carries of this adder are computed in parallel by two independent 4-bit carry chains. Implementation of wider adders based on the use of the proposed 8-bit adder module shows significant operating speed improvement compared to their corresponding adders based on the standard 4-bit MCC adder module.

The design of MCC adder circuits using conventional logic are summarized in sections II. The section III explains the architecture of

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double carry chain 8-bit MCC adders. The simulation results of MCC adder design using conventional logic styles and proposed logic style are compared in section IV and finally it is concluded in section V.

II. EXISTING LOGIC

Let us consider $A=a_{n-1}a_{n-2}\ldots a_1a_0$ and $B=b_{n-1}\ b_{n-2}\ldots\ B_1\ b_0$ represent two binary numbers to be added and $S=S_{n-1}S_{n-2}\ldots S_1S_0$ their sum. The symbols, +, $\oplus$, and − are used to denote the AND, Inclusive OR, Exclusive OR, and NOT logical operations, respectively. The addition of binary numbers, to compute the carry signals is based on the following recursive formula.

$$C_i=g_i+z_i.C_{i-1} \qquad (1)$$

Where, gi=ai.b_i and z_i are the carry generate and the carry propagate terms, respectively. In the case of Inclusive OR adders, is defined as $z_i=t_i=a_i+b_i$, while in the case of Exclusive OR adders, it is defined as $z_i=t_i=a_i\oplus b_i$. The implementation of the Domino generate and the Domino OR and XOR propagate signals are shown in figure.1.

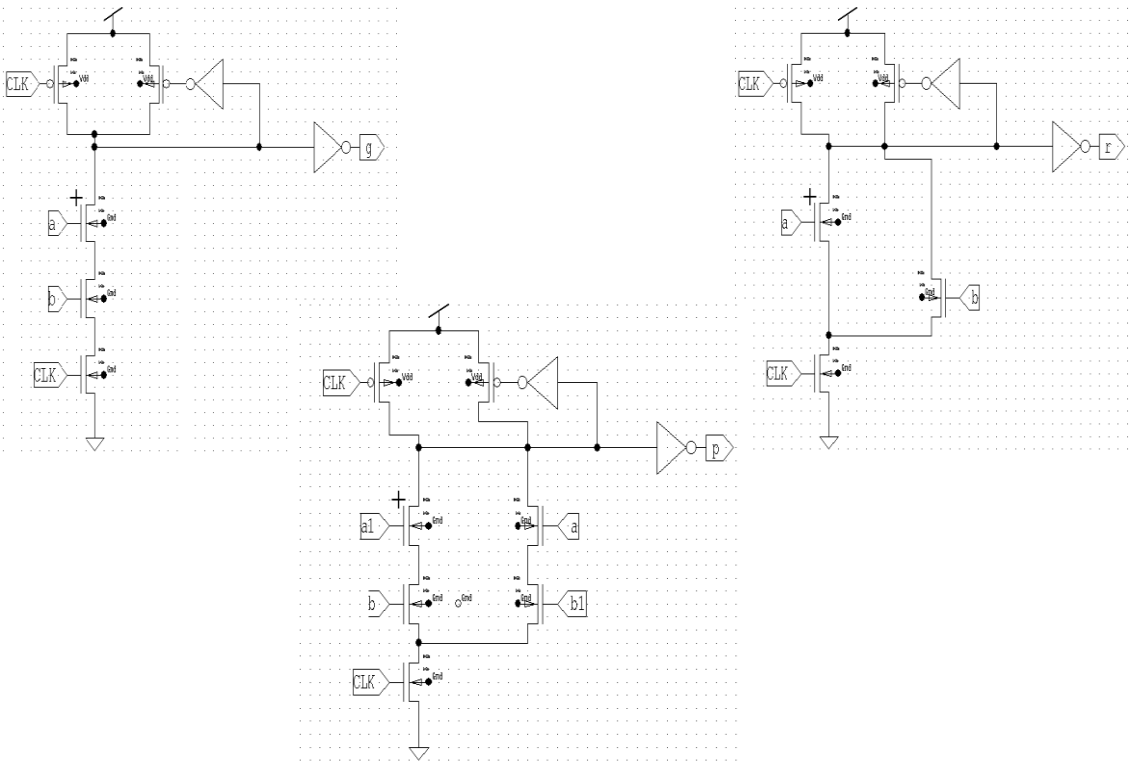

Figure 1. Domino implementation for the a) Generate b) Domino OR propagate c) Domino XOR propagate signals.

Equation (1) is expanded as follows.

$$C_i=g_i+z_i\ g_{i-1}+\ z_i\ z_{i-1}\ g_{i-2}+\ldots..\ z_i\ z_{i-1}\ldots\ z_1g_0+\ z_i\ z_{i-1}\ldots\ z_0C_{-1} \qquad (2)$$

The sum bits of the adder are defined as $Si=p_i\oplus C_{i-1}$, where C_{-1} is the input carry. The MCC generates all the carries computed according to relation (2) in parallel, using an iterative shared transistor structure. Practically, the CLA length is limited to four in order to cut down the number of series-connected transistors.

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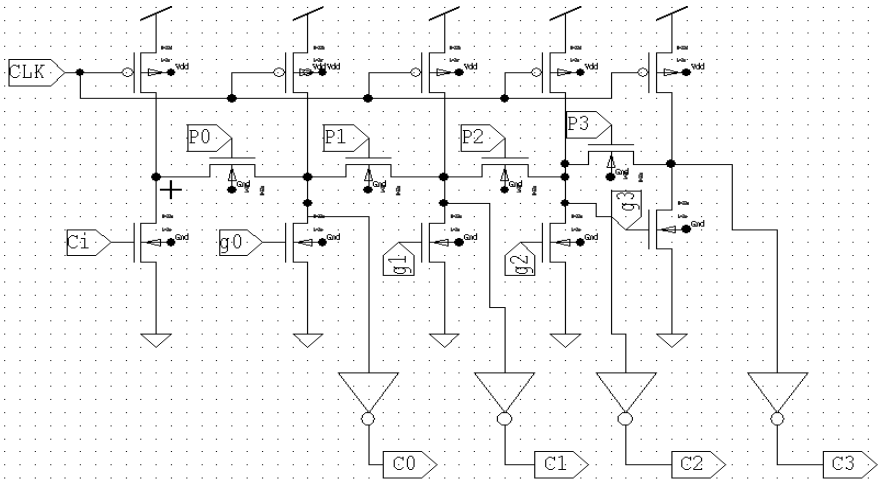

Figure.2 Conventional 4 bit Domino MCC

The implementation of the 4-bit carry chain using multioutput domino CMOS logic is shown in figure.2. The carry propagate signal is defined as $z_i=t_i=a_i+b_i$ to avoid false discharges reduced at the output nodes of the carry chain due to higher OR-AND forms of multioutput gates. To implement sum, the domino chain is terminated, and the sum bits of the MCC adder are the MCC is supported by the carry-skip capability to improve performance.

III. PROPOSED DOUBLE CARRY CHAIN ADDER

In an existing work, the length of their carry chains is limited to 4 bits due to the technological constraints. The Proposed design of an 8-bit MCC adder is implemented which is composed of two independent carry chains. These chains have the same length as the 4-bit MCC adders. The use of the proposed 8-bit adder as the basic block, instead of the 4-bit MCC adder, can lead to high-speed adder implementations. The implementation of the proposed double carry chain 8 bit MCC adder is shown in figure.4.

The derived here carry equations are similar to those for the Ling carries proposed in [11]–[13]. The derived carry equations allow the even carries to be computed separately of the odd ones. This separation allows the implementation of the carries by two independent 4-bit carry chains; one chain computes the even carries, while the other chain computes the odd carries. The design of the proposed 8-bit MCC adder is implemented in the following.

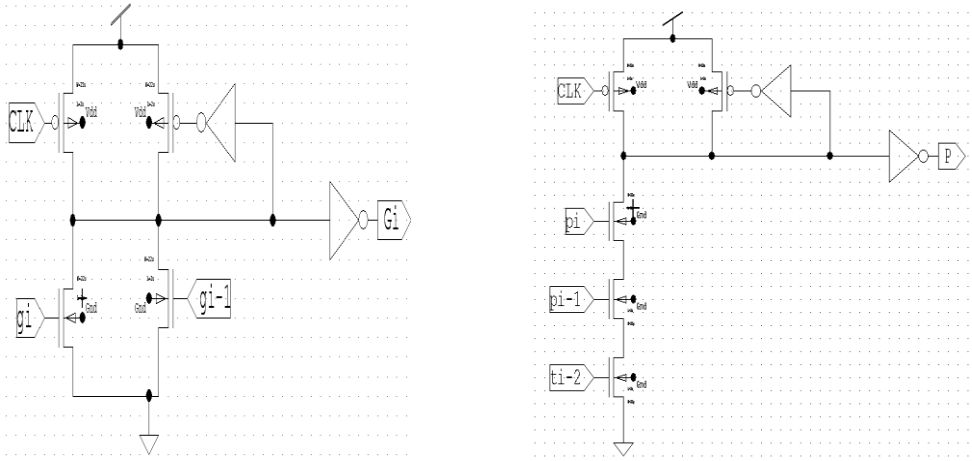

Figure.3 Proposed Domino a) Generate and b) Propagate signals.

(a) Computation of Even Carry:

For i=0 and $z_0=t_0$,

From the equation (1), then $c_0=g_0+t_0.c_{-1}$.

Since $g_i=g_i.t_i$, $c_0=t_0\ (g_0.c_{-1}) =t_0h_0$,

Where

$h_0= g_0+c_{-1}$ is the new carry.

From the equation (2),

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For i=2 and $z_i=p_i$,

$c_2= C_2=g_2+p_2g_1+ p_2p_1g_0+p_2p_1p_0c_{-1}$

Since $g_i+p_i.g_{i-1}=g_i+t_ig_{i-1}$ and $p_i= p_it_i$,

$c_2= t_2 (g_2+g_1+ p_2 p_1 g_0+ p_2 p_1 p_0c_{-1})$

$= t_2 (g_2+g_1+ p_2 p_1 t_0 (g_0+c_{-1})) =t_2.h_2$

Where

$h_2= g_2+g_1+ p_2p_1t_0 (g0+c_{-1})$ is the new carry.

Similarly, h_4, h_6 values are computes as follows,

$h_4= g_4+g_3+ p_4p_1t_2 (g_2+g_1+ p_2p_1t_0 (g0+c_{-1}))$

$h_6= g_6+g_5+ p_6p_5p_4t_2 (g_4+g_3+ p_4p_1t_2 (g_2+g_1+ p_2p_1t_0 (g0+c_{-1})))$

(b) Computation of Odd Carry:

The odd carries for the values of i are computed according to the aforementioned methodology proposed for the even carries as follows.

$h_1= g_1+g_0+p_1p_0c_{-1}$

$h_3= g_3+g_2+p_3p_2t_1 (g_1+g_0+p_1p_0c_{-1})$

$h_5= g_5+g_4+ p_5p_4t_3 (g_3+g_2+p_3p_2t_1 (g_1+g_0+p_1p_0c_{-1}))$

$h_7= g_7+g_6+ p_7p_6t_4 (g_5+g_4+ p_5p_4t_3 (g_3+g_2+p_3p_2t_1 (g_1+g_0+p_1p_0c_{-1})))$

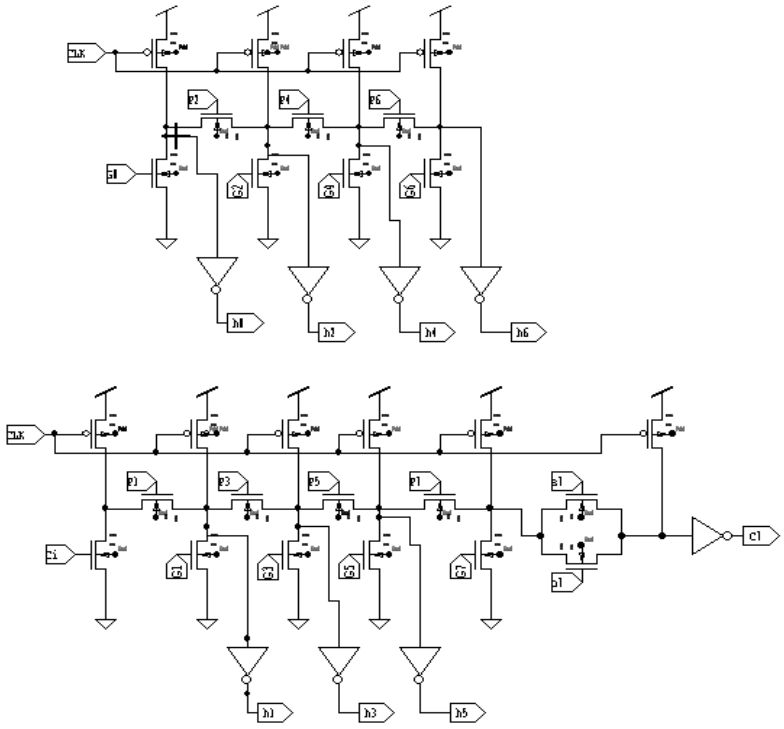

Figure.3 Proposed Double Carry Chain 8 bit MCC Adder

Let $G_i= g_i+g_{i-1}$ and $Pi= p_i+p_{i-1}$ be the new generate and propagate signals respectively, where, $g_{-i}=c_{-1}$ and $t_{-1}=1$. Then the equation is derived as follows.

For even values of i,

h2 =G2 + P2G0

h4 =G4 + P4G2 + P4P2G0

h6 =G6 + P6G4 + P6P4G2 + P6P4P2G0

While for odd values of I,

h1 =G1 + P1c−1

h3 =G3 + P3G1 + P3P1c−1

h5 =G5 + P5G3 + P5P3G1 + P5P3P1c−1

h7 =G7 + P7G5 + P7P5G3 + P7P5P3G1 + P7P5P3P1c−1.

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IV. SIMULATION RESULTS AND DISCUSSION

The proposed 8 bit MCC adder and the conventional adder are designed in a 0.18-μm CMOS technology. The propagation delay, power consumption, and power-delay product are obtained at the supply voltage of 1.8 V. Due to the technological constraints, the length of the carry chains of conventional adder is limited to 4 bits. The proposed 8 bit double carry chain adder has a significantly reduced propagation delay compared to the conventional adder. The obtained simulation results for conventional and proposed adders are summarized in Table.1.

Table.1 Comparison Results of Conventional and Proposed Adders

Parameter	**Power Delay Product (Ws)**				
Logic	**8 bit MCC Adder**	**16 bit MCC Adder**	**32 bit MCC Adder**	**64 bit MCC Adder**	**128 bit MCC Adder**
Existing Method	$1.838\text{x}10^{-7}$	$3.662\text{x}10^{-7}$	$7.308\text{x}10^{-7}$	$1.458\text{x}10^{-6}$	$2.918\text{x}10^{-6}$
Proposed Method	$1.267\text{x}10^{-7}$	$2.524\text{x}10^{-7}$	$5.042\text{x}10^{-7}$	$1.008\text{x}10^{-6}$	$2.05\text{x}10^{-6}$

V. CONCLUSION

The proposed 8-bit MCC adder in multi output domino CMOS logic is designed using 180nm technology. The MCC is an efficient and widely accepted design approach to construct CLA adders. The proposed logic style is based on two independent 4-bit carry chains. Due to its limited carry chain length, the use of the proposed 8-bit MCC carry chain adder leads to significant operating speed improvement then compared to the corresponding adders based on the standard 4 bit adder module. module for the implementation of wider adders leads to significant operating speed improvement compared to the corresponding adders based on the standard 4-bit MCC adder module. The 8-, 16-, 32-, 64-, and 128-bit adders using both conventional and proposed logics are also implemented in 180nm technology. The simulated results show that the Power-Delay Product of the proposed design is less compared to the conventional design.

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