



ISBN	978-81-929742-6-2
Website	icieca.in
Received	02 - April - 2015
Article ID	ICIECA024

VOL	01
eMail	icieca@asdf.res.in
Accepted	15 - November - 2015
eAID	ICIECA.2015.024

FPGA Digital Data Acquisition with Rate Buffering for X-ray Sensor for XSM payload of Chandrayaan-2

Priyanka D Goswami¹

¹Instrumentation and Control Engineering,
 Institute of Technology, Nirma University
 Ahmedabad, Gujarat

Abstract: The XSM is one of the proposed sensors for the Chandrayaan-2 satellite. It measures the X-ray spectrum of solar x-ray. The paper discusses a UART based digital data acquisition system that consists of three modules: the clock generator block, the ADC interface block that converts the 16 bit data to 8 bit data and the UART module that transmits the data in serial form using RS232 protocol with start and stop bits. The programming is done using Verilog language in Libero IDE software. The testing is done using ModelSim. The UART has been developed in the Actel ProAsic 3 FPGA.

Keywords: XSM, Chandrayaan-2, ModelSim.

INTRODUCTION

Solar X-ray Spectrometer (XSM) is one of the proposed sensors for the Chandrayaan-2 satellite (orbiter), which will be launched in the near future by ISRO, India. This sensor will provide measurement of X-ray spectrum of solar X-rays in the energy range of 1- 20 keV with energy resolution of approximately 200eV at 5.9 keV. XSM instrument will be made up of the sensor package and the electronics package. The detector analog output will be pre-processed for event detection, and then converted to digital form using 10 bit ADC, which will be processed further in a FPGA (Field Programmable Gate Array)^[1]. The digital data stream will be transferred to the satellite data transmission electronics for sending it to Earth stations.

Here I describe a FPGA based Digital Data Acquisition Subsystem (DDAS), which receives the XSM ADC digitized word stream, provides a simple rate buffering and then an output serial stream with UART format. All components of the DDAS, including the UART convertor are designed, developed and implemented within a Pro-ASIC Actel FPGA.

XSM Instrument- Brief

The X-ray radiation will be detected by a silicon drift detector, which provides a very fast response and a wide dynamic range. The detector will have a suitable window and cover to provide the threshold limit for high energy X-rays up to 1 keV. It will be also covered with an aluminum cap, very close, which will provide it a wide field of view. Additionally protection covers from intense and sudden solar X-ray bursts will be incorporated. This sensor module will be mounted on a bracket outside the satellite. Signals from the sensor will be brought out, and transferred to the XSM electronics module, in the satellite. Temperature of the sensor module is maintained using a temperature controller. Electronics processing circuits include sensor signal pre-processing using pre-amplifiers, peak detection and Analog to Digital conversion (10 bit). The raw data rate from the ADC, is such that after the post processing, the instrument will generate 1024 channel energy spectrum information per second^[1]. The processed digital data is formatted and transferred to the payloads data processing unit.

This paper is prepared exclusively for International Conference on Innovative Trends in Electronics Communication and Applications 2015 [ICIECA] which is published by ASDF International, Registered in London, United Kingdom. Permission to make digital or hard copies of part or all of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage, and that copies bear this notice and the full citation on the first page. Copyrights for third-party components of this work must be honoured. For all other uses, contact the owner/author(s). Copyright Holder can be reached at copy@asdf.international for distribution.

2015 © Reserved by ASDF.international

Cite this article as: Priyanka D Goswami. "FPGA Digital Data Acquisition with Rate Buffering for X-ray Sensor for XSM payload of Chandrayaan-2". *International Conference on Innovative Trends in Electronics Communication and Applications (2015)*: 166-169. Print.

FPGA DIGITAL DATA ACQUISITION SYSTEM

FPGA Digital Data Acquisition System

A system for acquiring the raw SDD digitized (10bit) data, with a simple computer interface is required, during the development and testing of the XSM sensor. The raw data rate is higher than the final sensor data rate and it can be of the variable rate. Further it should have the minimum devices and simple operation. Hence the design of the DDAS was carried out such that, it could be incorporated within the Actel Pro-Asic FPGA device that was used to interface with the ADC circuit board. The output was required on a commonly available I/O port in any desktop computer, with minimum wiring connections, and with default software drivers on the computer. To meet with these, the DDAS was designed with a front end data buffering register set with the control signals driven by the ADC, a serial to parallel convertor with direct formatting for UART/RS-232c serial format connected to a buffered output pin of FPGA to drive the serial data to a computer RS-232 port.

This design does not require any external UART or USB interface device, and thus reduces the complexity, while also removing the need to provide FPGA logic, required to initialize and control such special devices, which also requires involved HDL programming, special UART device control/programming lines. At the same time, it only provides that RS-232 functionality subset which is required for this application. The goal is continuous data acquisition with the above scheme by selecting a UART transmission rate at least two times faster than the input data rate.

Design and Implementation Method

Design and HDL coding was carried out using Verilog, using the Libero project environment, natively used for the Actel Pro-Asic devices. The code simulation and verification was done using Modelsim (in built in Libero). The Steps followed for the design, development and simulation of DDAS are shown in figure.1.

Some of the features and facilities in Libero, used to implement the project were:

- Project and design flow management
- Synplify Pro ME synthesis which optimizes Actel FPGA device performance and area utilization.
- Modelsim ME VHDL or Verilog behavioral, post-synthesis and post-layout simulation.
- Physical design implementation and I/O pin layout.
- Interface for device programmer.

Modular approach was followed for DDAS design, with each module implementing a specific function and connected to other modules with defined electrical and timing interfaces. This resulted in ease of simulation and testing the DDAS. The modules are (1) Clock generator (2) ADC interface and register set for initial rate buffering (3) Parallel word to serial and UART formatting along with serial output.

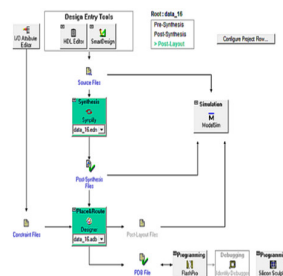


Figure. 1. Flowchart showing steps of project development in Libero IDE

Each module is briefly described,

- Clock Generator was created to give the desired clock rate to the UART block. The block would use the 40MHz FPGA clock as the input and using a frequency divider reduce the clock frequency to standard frequency required by the UART for data transmission.

Cite this article as: Priyanka D Goswami. "FPGA Digital Data Acquisition with Rate Buffering for X-ray Sensor for XSM payload of Chandrayaan-2". *International Conference on Innovative Trends in Electronics Communication and Applications (2015)*: 166-169. Print.

- The ADC Interface module took the input, 16 bit data from the ADC (Analog to Digital Converter). This data is divided into two 8 bit words (MSB and LSB) and transmitted over to the UART block, along with necessary timing signals. This is required as UART can send maximum 8 bit data (excluding start and stop bits) in one cycle.
- UART module in which the 8 bit parallel data received from the above block is transmitted serially and the output can be taken from the assigned I/O pin of the FPGA and given to the RS232 port of PC for data transmission. Hence this block will basically act as a parallel to serial data converter with the ADC 8 bit byte (part of the Word) inserted into the UART work register at the required bit locations. The output data packet for each input byte will be of 11 bits (1 start bit, 8 bit data, and 2 stop bits) and this will be transmitted serially.

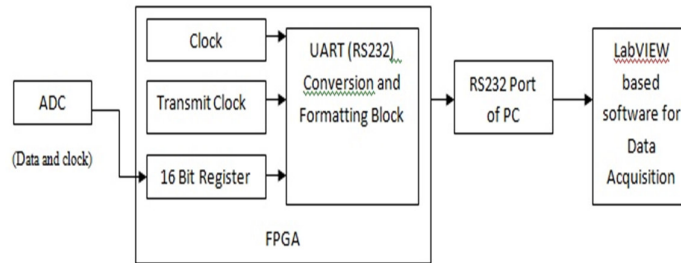


Figure.2. Block Diagram of DDAS module

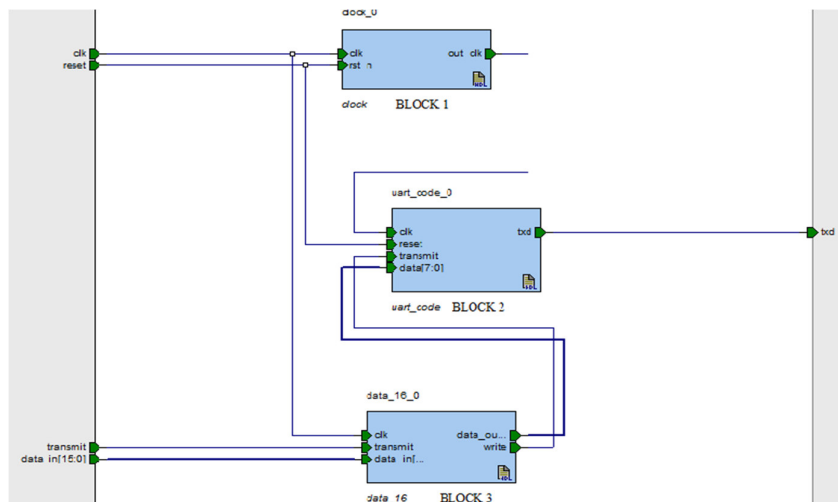


Figure.3 Design flow of the blocks (LiberoIDE software)

Simulation and Testing

Each block was created compiled and simulated in th Libero IDE software using tools such as HDL Editor, SySnplify and ModelSim. The simulation was carried out for different UART bit rates like 76 kbits and 115 kbits. Microsemi FlashPRO module was used to load the HDL code in the FPGA and the output was observed on the DSO.

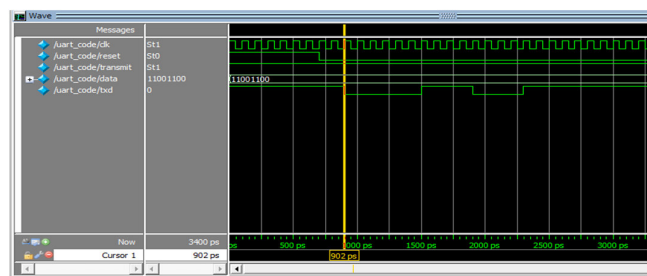


Figure.4. Output waveforms of UART using ModelSim

Cite this article as: Priyanka D Goswami. "FPGA Digital Data Acquisition with Rate Buffering for X-ray Sensor for XSM payload of Chandrayaan-2". *International Conference on Innovative Trends in Electronics Communication and Applications (2015)*: 166-169. Print.

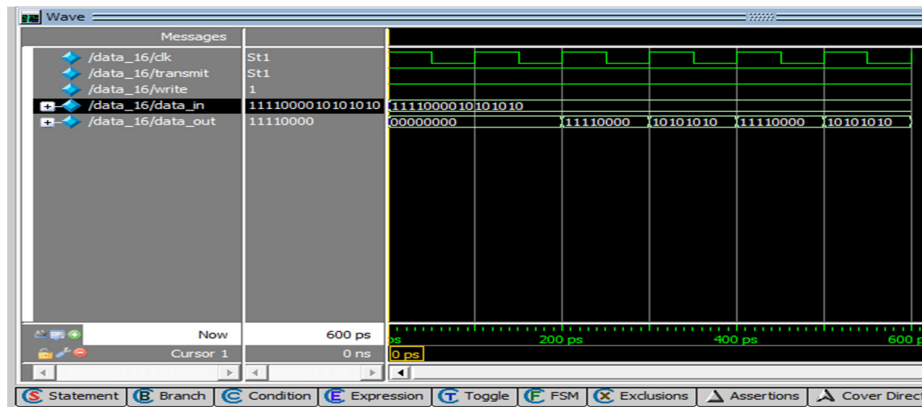


Figure.5. Output waveforms of 16 bit to 8 bit convertor using ModelSim

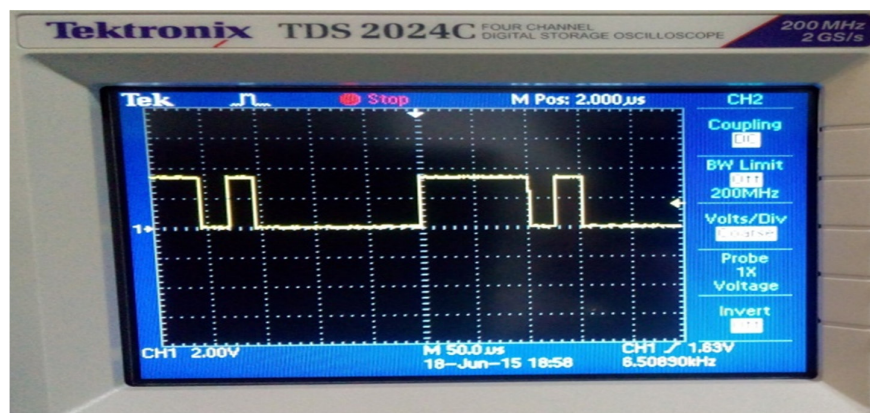


Figure.6. Waveform of 11 bit serial output for 8 bit parallel input data given to UART (as seen on DSO)

CONCLUSION

The DDAS with a UART serial data interface, compatible with the XSM detector digitized data stream was designed, developed and tested with the Actel Pro-Asic FPGA.

ACKNOWLEDGMENT

I would like to convey my gratitude to Mr. M Shanmugam, Sr. Scientist,PRL,DOS, for providing me with the opportunity to work at the PLANEX laboratory, and for guiding me throughout the project. I would also like to thank Mr. Arpit Patel, Mr.Tinkal Ladiya and the other staff members for helping me, guiding me and providing the required resources for the successful completion of the project. I am also thankful to the Dean, Physical Research Laboratory, DOS, and Ahmedabad for granting me the opportunity to work at this prestigious institution.

REFERENCES

- [1] Real World FPGA Design with Verilog by Ken Coffman, Prentice Hall PTR
- [2] M. Shanmugam, S. Vadawale, Y. B. Acharya, S. K. Goyal, Arpit Patel, Bhumi Shah and S. V. S. Murty "Solar X-ray Monitor (XSM) on-board Chandrayaan-2 orbiter" 43rd Lunar and Planetary Science Conference, March 2012, LPI Contribution No. 1659, id. 185
- [3] Computer Arithmetic and Verilog HDL Fundamentals by Joseph Cavanagh, CRC Press
- [4] Actel ProAsic [Online] www.microsemi.com

Cite this article as: Priyanka D Goswami. "FPGA Digital Data Acquisition with Rate Buffering for X-ray Sensor for XSM payload of Chandrayaan-2". *International Conference on Innovative Trends in Electronics Communication and Applications (2015)*: 166-169. Print.