A New Hybrid 9-Level Cascaded H-Bridge Multi Level Inverter for Low Power Applications

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Abstract: Multilevel converters offer advantages in terms of the output waveform quality due to the increased number of levels used in the output voltage modulation. This advantage is particularly true for cascade H-bridge (CHB) converters that can be built to produce a large number of levels owing to their modular structure. When increase the number of levels it requires more number of switches, it implies the size and cost of the device increases. To overcome this problem here we present a new Hybrid Cascaded H-Bridge Multi Level Inverter with reduced number of switches, this Hybrid Cascaded H-Bridge MLI is effective & efficient in improving the quality of the inverter output voltage as well as the output Power. Here, we describe about the structural parts, switching strategy and operational principles of the Hybrid Cascaded H-Bridge MLI. The Proposed topology reduces the number of switches as well as the number of Pulse generators. The simulation is done in MATLAB/SIMULINK software and the results shown for the existing multilevel inverter & proposed multilevel inverter, THD is reduced and also better speed response.

Keywords: Multi Level Inverter (MLI), Cascaded H-bridge, THD, Multi Level DC Link (MLDC), MATLAB/ SIMULINK Software.

1. Introduction

Multilevel inverter (MLI) structures have been developed to overcome shot comings in solid states switching device rating so that they can be applied to high voltage electrical systems. The multilevel; voltage source inverters unique structure allows them to reach high voltages with low harmonics without the use of the transformers. This makes these unique power electronics topologies suitable for flexible ac transmission system (FACTS) and custom power applications. The use of multilevel inverter to control the frequency, voltage output (including the phase angle), and real and reactive power flow dc/ac interface provides significant opportunities in the control of distributed power systems.

The multilevel topologies can be classified into three main categories: the neutral point clamped (NPC) [1], the flying capacitors [2] and the cascade H-bridge (CHB) converters [3]. The three-level NPC bridge is probably the most widely used topology for medium-voltage ac motor drives and pulse width modulation (PWM) active rectifiers [4]. NPC converters with more levels are also possible, although there are significant problems in the balancing of their dc- link capacitor voltages [5] unless modified modulation strategies [6] or an additionally circuitry [7] is used. On the other hand, the CHB converter is normally implemented with a large number of levels but at the cost of complicated and bulky input transformers with multiple rectifiers [8] or multi winding three-phase output transformers [9]. For this reason, in applications with no active power transfer, such as in reactive power compensation, where the converter can operate without the rectifier front end, the CHB is a highly attractive solution [10].

Multilevel inverters have recently increased interest in the research and industry communities in these kinds of inverters, the output voltage can take several discrete levels of equal magnitude. The multilevel inverters are aimed at reducing the harmonic content of generated voltage or current waveforms. The harmonic content of such a waveform is greatly reduced, if compared with a two-level waveform.

As the number of voltage levels m grows the number of active switches increases according to 2(m-1) for the existing cascaded H-bridge multilevel inverters. This project presents a nine level cascaded H-bridge multilevel inverter based on a Multilevel DC Link (MLDCL) and a bridge inverter. Compared with the existing cascaded multilevel inverters, the cascaded MLDCL inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. For a given number of voltage levels m, the cascaded MLDCL inverter requires m+3 active switches, roughly half the number of switches Simulation results are included to verify the operating principle of the proposed MLDCL inverters.

2. Multilevel Inverter

The voltage source inverters produce an output voltage or current with levels either 0 or ±Vdc. They are known as the two-level inverter. To produce a quality output voltage or a Current wave form with less amount of ripple content, they require high switching frequency. In high- power and high voltage applications these two level inverters, however, have some limitations in operating at high frequency mainly due to switching losses and constraints of device ratings. These limitations can be overcome using multilevel inverters. The multilevel inverters have drawn tremendous interest in power industry. It may be easier to produce a high-power, high voltage inverter with multi-level structure because of the way in which the voltage stresses are controlled in the structure. The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics without use of transformers or series connected synchronized-switching devices. As the number of voltage levels increases, the harmonic content of the output voltage wave form decreases significantly.

The multilevel inverter consists of series connection of switching power devices and each device is clamped to the dc link capacitor voltage through the clamping diodes, it does not require special consideration to balance the voltages of the power devices. In a multilevel inverter, each device is stressed to a voltage $V_{dc}/(n-1)$ where n is the number of levels and V_{dc} is the dc bus voltage. Hence the device stress is considerably reduced as the number of levels increases. This makes the multi-level inverters a best choice for the high voltage and high power applications and hence drawn a lot of attention for high power industrial applications.

The most attractive features of multilevel inverters are 1. They can generate output voltages with extremely low distortion and low dv/d t. 2. They draw input current with extremely low distortion. 3. High Efficiency.
A. Cascaded H-Bridge MLI: A single-phase structure of an m-level cascaded inverter is illustrated in Figure.

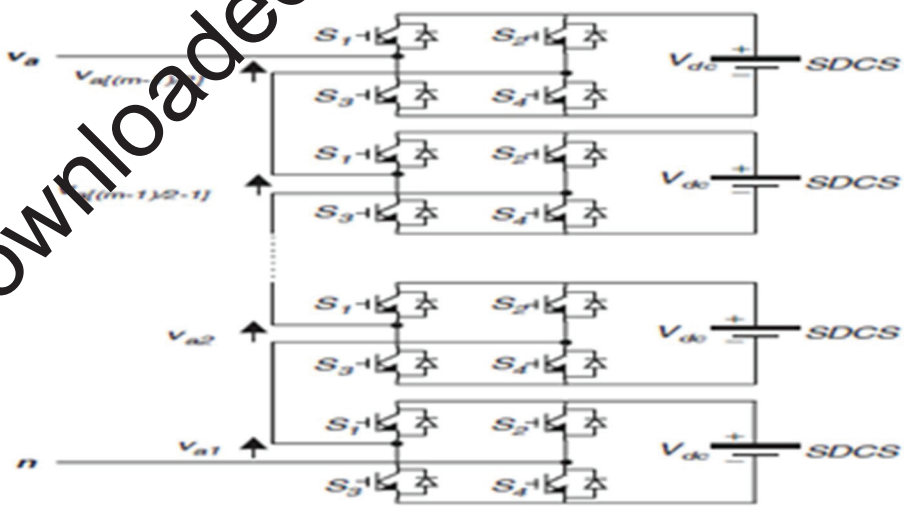

Fig. 1. Single-phase structure of a multilevel cascaded H-bridge Inverter

Table1.Switching Sequence for five levels Cascaded H-Bridge MLI

Switches / Output voltage	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
0 V	1	0	1	0	1	0	1	0
1V	1	0	1	0	1	1	0	0
2 V	1	1	0	0	1	1	0	0
1V	1	1	0	0	0	1	0	1
0 V	0	1	0	1	0	1	0	1
-1V	0	1	0	1	0	0	1	1
-2 V	0	0	1	1	0	0	1	1
0 V	0	0	1	1	1	0	1	0

Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4. To obtain $+V_{dc}$, switches S1 and S4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S2 and S3. By turning on S1 and S2 or S3 and S4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by $m = 2s+1$, where s is the number of separate dc sources.

3. Proposed Hybrid Multilevel Inverter Scheme

The proposed cascaded H-bridge MLDCL inverter topology consists of a multilevel DC source to produce DC-link bus voltage V_{bus} and a single-phase full-bridge (SPFB) inverter consists of four switches S1-S4 to alternate polarity of DC-link bus voltage to produce an AC voltage. The DC source is formed by Connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two switches S_{ak} and S_{bk}. The two switches and operate in a toggle fashion. The cell source is bypassed with S_{ak} on and S_{bk} off, or adds to the dc link voltage by reversing the switches. Figure.2 shows a circuit diagram of the proposed cascaded H-bridge MLDCL inverter topology.

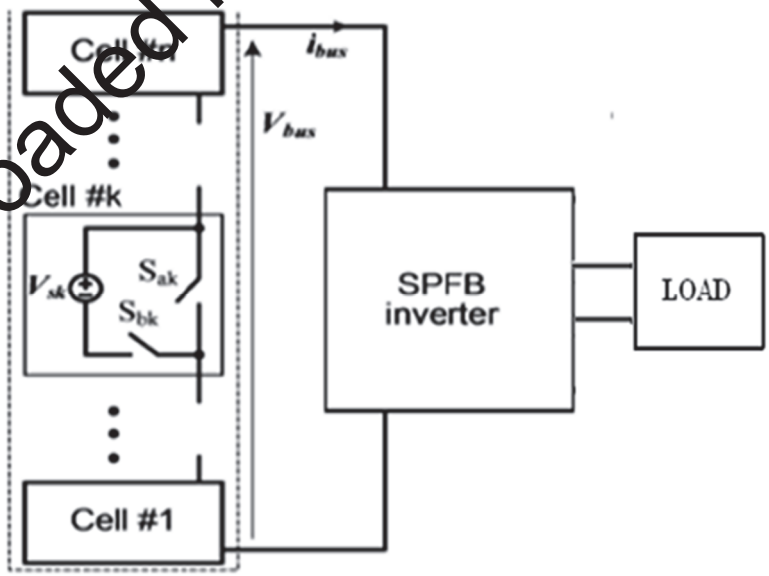

Fig.2 Block diagram of Proposed Hybrid MLI

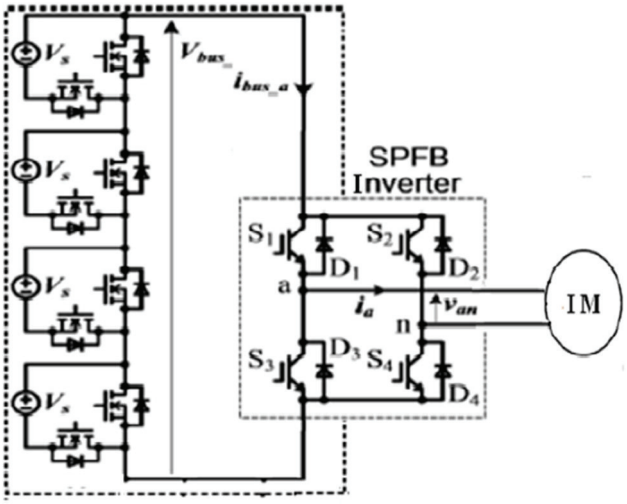

Fig.3 Circuit diagram of Proposed Hybrid MLI

The circuit diagram of the cascaded H-bridge multilevel DC-link inverter topology shown in Figure.3, it consists of multilevel DC-link voltage source and single phase full bridge inverter.

Multilevel DC-link voltage source:

Multilevel DC-link voltage source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two IGBT switches as shown in the Figure 4.

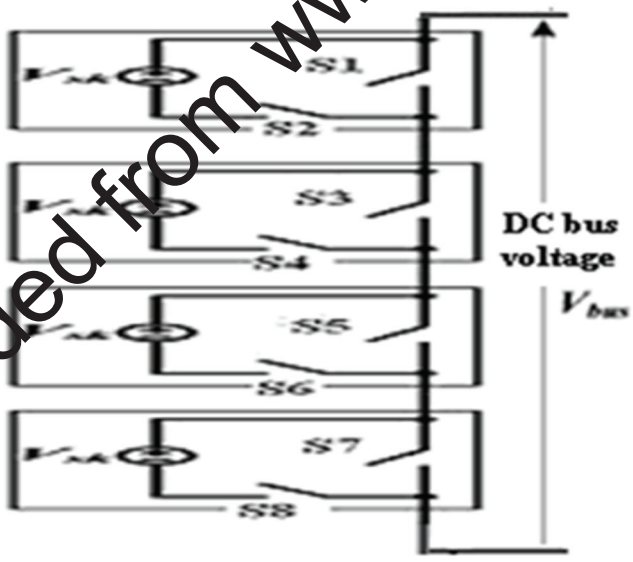

Fig.4 MLDCL Voltage source

The two IGBT switches will operate in a toggle fashion. Low on resistance and fast switching capability, low voltage IGBTS are utilized in each cell source to reduce the inverter cost or to provide a high bandwidth sinusoidal output voltage. The IGBT switches are triggered by proper switching signals to produce multi level DC-link bus voltage which is indicated by Vbus in the circuit diagram. Various modes of switching sequence is given in the table 2 to produce DC bus voltage Vbus with the shape of stair case with (n=4) steps, where n is the number of cell source that is given to the SPFB inverter.

Table2.Various modes of switching sequence to produce DC bus voltage

MODE 1	MODE 2	MODE 3	MODE 4	MODE 5
S1-ON S2-OFF	S2-ON S1-OFF	S2-ON S1-OFF	S2-ON S1-OFF	S2-ON S1-OFF
S3-ON S4-OFF	S3-ON S4-OFF	S4-ON S3-OFF	S4-ON S3-OFF	S4-ON S3-OFF
S5-ON S6-OFF	S5-ON S6-OFF	S5-ON S6-OFF	S6-ON S5-OFF	S6-ON S5-OFF
S7-ON S8-OFF	S7-ON S8-OFF	S7-ON S8-OFF	S7-ON S8-OFF	S8-ON S7-OFF
MODE 6	MODE 7	MODE 8	MODE 9	
S2-ON S1-OFF	S2-ON S1-OFF	S2-ON S1-OFF	S1-ON S2-OFF	
S4-ON S3-OFF	S4-ON S3-OFF	S3-ON S4-OFF	S3-ON S4-OFF	
S6-ON S5-OFF	S5-ON S6-OFF	S5-ON S6-OFF	S5-ON S6-OFF	
S7-ON S8-OFF	S7-ON S8-OFF	S7-ON S8-OFF	S7-ON S8-OFF	

By giving the switching pulses to the switches in four H-bridge cells the MLDCL voltage source produces DC bus voltage Vbus with the shape of stair case with (n=4) steps that approximates the rectified waveform of the commanded sinusoidal voltage, where n is the number of cell sources that is given to the SPFB inverter. The desired DC bus Voltage Vbus is shown in the Figure 5.The switches in four cells will operate at twice of the fundamental frequency of the output voltage.

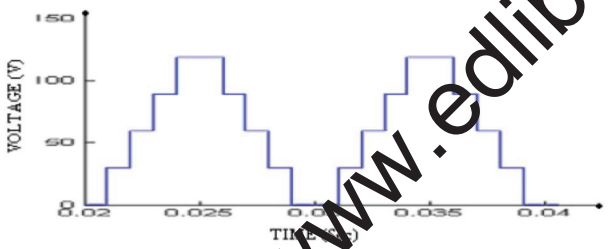

Fig 5.Desired DC bus voltage Vbus of cascaded H-bridge MLDCLI

Principle of Operation of Nine Level Cascaded H-bridge MLDCL Inverter

The principle of operation of nine level cascaded multilevel DC-link inverter is explained by explaining the operating principles of multilevel DC link voltage source and single phase full bridge inverter. To produce nine level AC output voltage Van the multilevel DC-link source is formed by connecting four H-bridge cells in series with each cell having a separate voltage source controlled by two switches Sak and Sbk which will operate in a toggle fashion. The cell source is bypassed with Sak on and Sbk off, or adds to the DC link bus voltage by reversing the switches. The DC bus voltage Vbus is fed to the SPFB inverter. The switching signals are given to the SPFB inverter in turn to alternate the voltage polarity of the DC bus voltage Vbus for producing an AC output voltage Van of a stair case shape with (2n+1)=9 levels, whose voltages are -(V1+V2+.....+ Vn) , -(V1+V2+.....Vn-1).....,-V2, - V1 ,0, V1, V2,.....(V1+V2+....Vn-1), (V1+V2+....Vn). Where V1,V2.....Vn are voltages of cell sources. The desired AC output voltage Van of cascaded H-bridge is shown in the Figure 6

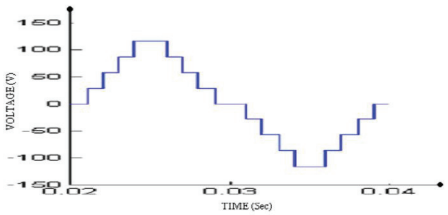

Fig.6 Desired AC output voltage Van of cascaded H-bridge MLDCL

4. Simulation Results

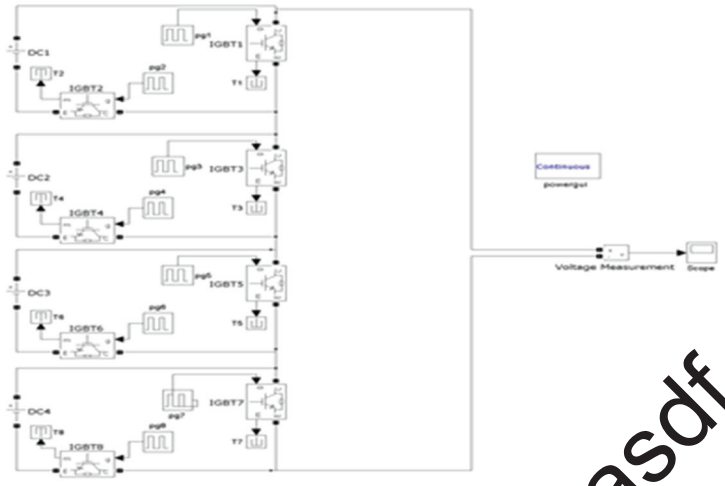

Fig.7 Proposed Nine level Cascaded H-Bridge MLDCL

Here demonstrated that the MLDCL inverters can significantly reduce the component count. As the number of voltage levels m grows, the number of active switches required is 2*(m-1) =16 for existing cascaded multilevel inverter and m+3 =12 switches are required for cascaded H bridge MLDCL inverter.
Here the simulation of conventional 9 level H bridge MLI and new proposed 9 level Cascaded H bridge MLDCL had done with RL load and Induction Motor (IM), and both the results are shown here

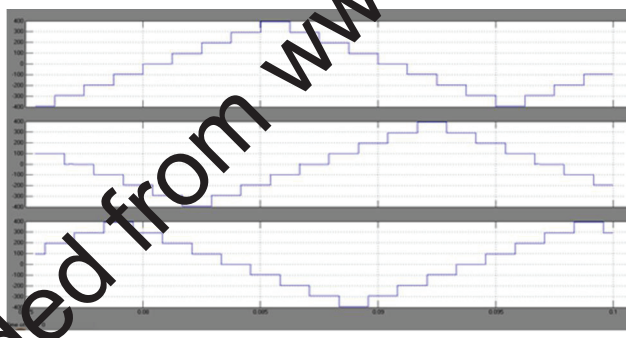

Fig.8 Simulation results of 9 level Cascaded H-Bridge MLI

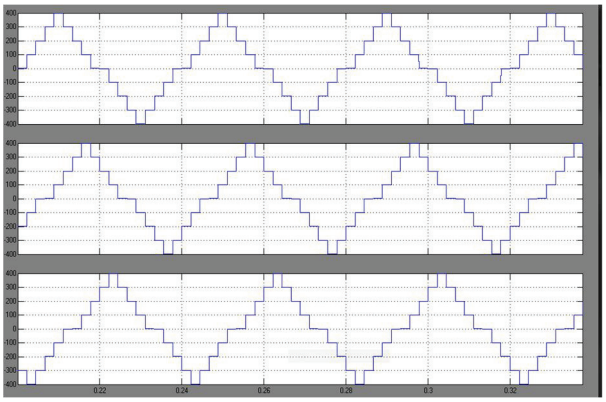

Fig.9 New proposed 3 phase Cascaded H-Bridge MLI output waveforms

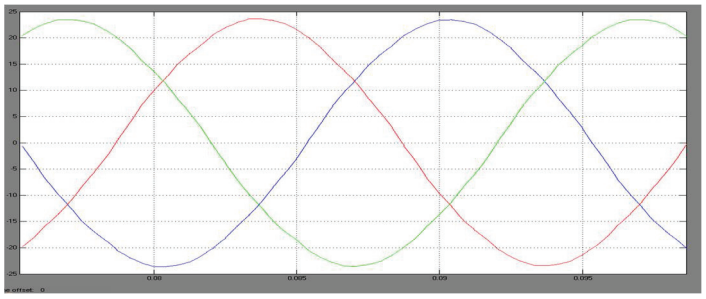

Fig.10 3-phase output current wave forms of 9 level conventional MLI fed IM

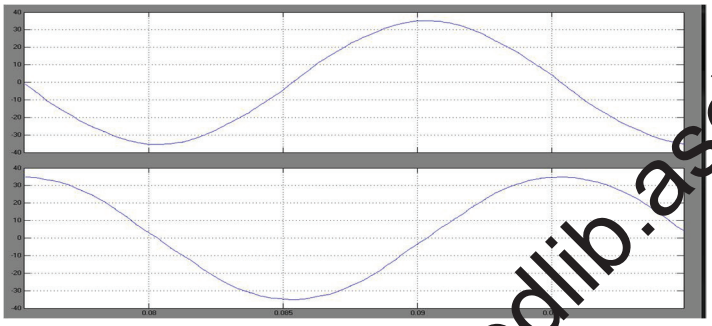

Fig.11 Currents I_{ds} & I_{qa} waveforms of 9 level conventional MLI fed IM

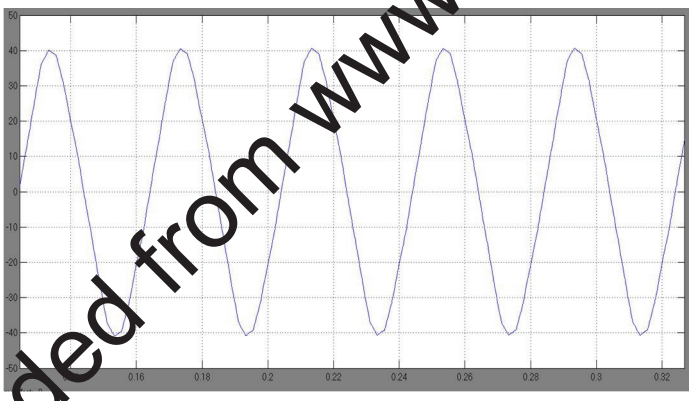

Fig.12 Output current of new proposed Three phase Cascaded H-Bridge MLI fed IM

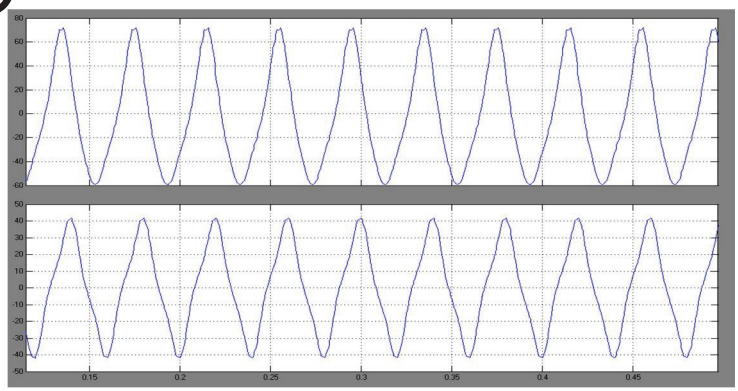

Fig.13 Currents I_{ds} & I_{qa} waveforms of new proposed 9 level conventional MLI fed IM

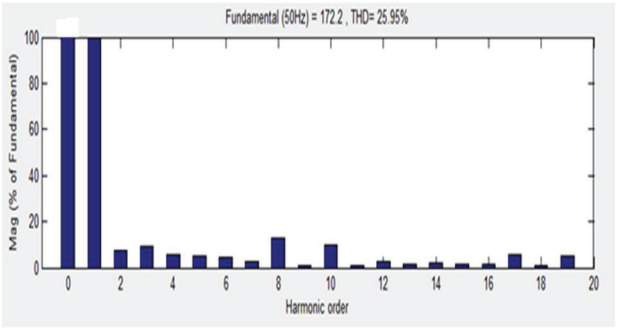

Fig.14 THD waveform for 9 Level conventional Cascaded H-Bridge MLI

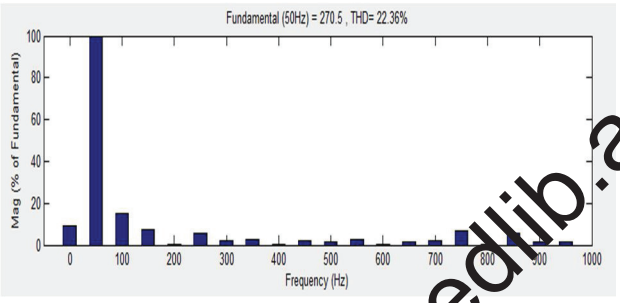

Fig.15 THD waveform for New proposed 9 Level Cascaded H-Bridge MLI

Fig 14 & Fig 15 are shown the Total Harmonic Distortion of 9 Level conventional Cascaded H-Bridge MLI and for New proposed 9 Level Cascaded H-Bridge MLI, from the above THD values we can observe that the THD value of New proposed 9 Level Cascaded H-Bridge MLI got less value compared to 9 Level conventional Cascaded H-Bridge MLI

Conclusion

Despite a higher total VA rating of the switches, the cascaded MLDCL inverters are cost less due to the savings from the eliminated gate drivers and from fewer assembly steps because of the substantially reduced number of components, which also leads to a smaller size and volume. One application area in the low-power range (100 kW) for the MLDCL inverters is in permanent-magnet (PM) motor drives employing a PM motor of very low inductance. The MLDCL inverter can utilize the fast-switching low-cost low voltage MOSFETs in the half-bridge cells, and the IGBT's in the single-phase bridges to dramatically reduce current and torque ripples and to improve motor efficiency by reducing the associated copper and iron losses resulting from the current ripple. These configurations may also be applied in distributed power generation involving fuel cells and photovoltaic cells.

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