Design of Analog Front-End for 128 Multi-Channel EEG Signal Acquisition in 90nm Technology

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Abstract - **This paper presents the design and implementation of a fully differential analog front-end which pre-processes the acquired Electro Encephalogram (EEG) signals before digitization. It consists of an analog multiplexer and a filter which can efficiently condition real-time EEG signals. The circuit has been designed so as to be compatible with a 128 multi-channel data acquisition system and hence, a 128 multi-channel analog multiplexer has been designed which aids in selecting the signal to be processed. Further, EEG signals are known to exist in the frequency range of 0-5 KHz and amplitude range of 100nv to 10mv. Hence, an eighth order low-pass filter with a bandwidth of 5 KHz, a stop band attenuation of -105dB, and a pass-band gain of 35.56dB has been implemented using cascaded bi-quads. The entire filter possesses fully-differential architecture because of its ability to effectively suppress power-line interference and on-chip noise. Chebyshev implementation of Ackerberg-Mosseberg bi-quad helped in conserving the chip area and aided in effective noise suppression. The schematics of the above mentioned circuits have been simulated in the 90nm technology.**

I. INTRODUCTION

The electrical signals generated due to the cumulative action potentials of the neurons, have, over the years provided an insight into the functioning of the brain. These signals, acquired through strategically placed electrodes either invasively or non-invasively, comprises of the EEG [4-7]. It is challenging to acquire invasive EEG signals and thus, noninvasively acquired EEG signals are more popular [4-7]. But, these signals have to be thoroughly pre-processed through strict filtering before they can be sampled, digitized and stored on-chip.

A block diagram of the pre-processing system and the components adjoining it, is shown in Fig.1. There are 128 electrodes placed spatially on the scalp to allow analysis of signals from different parts of brain. So, a 128 channel input multiplexer is designed to facilitate selection of any one of the 128 channels as the input to the filter. This filter's output is then fed to a sigma-delta ADC which gives out a 24-bit quantized signal. These signals can be processed and are used

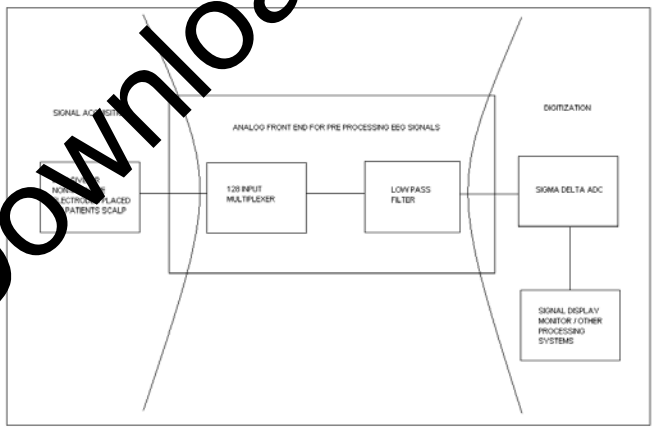

Fig.1. Block Diagram of the System to diagnose several brain disorders and diseases.

As most of the neural activity occurs in the lower frequencies, it is aimed to design a low-pass filter with a cut off of 5 KHz [5]. The voltage range of the neural EEG signals is typically 100nV to 10mv [5]. The minimum voltage that needs to be resolved is 100nv, which when digitized needs 24 bits to be represented. Each bit in the resolution results in a -6dB/octave roll-off, hence we need a -140 dB/decade roll-off. Since the input voltages of the ADC are in the range of 600mV rail to rail, it is required to implement the filter with a gain of 35.56dB or 60V/V. The number of electrodes to be used is 128. Hence, it conditions to have a 128 multi-channel multiplexer.

The filter design is done in a bottom-up process. Initially, single stage operational amplifier (Op-Amp) and two stage Op-Amp are designed using telescopic Op-Amp with gain boosted first stage and a common source second stage. Ackerberg-Mossberg bi-quad uses ideal Op-Amp's cascaded in inverting and non-inverting configurations with a feedback using appropriate resistors and capacitors, providing required gain. In order to approximate the behaviour of designed Op-Amp's to the behaviour of ideal Op-Amp's, a tolerance of 1% in the transfer function is allowed. MATLAB simulations have been done and a gain of 40dB for single stage Op-Amp and a gain of 60dB for two stage Op-Amp are fixed as ideal Op-Amp's. A cascade of four Ackerberg-Mossberg bi-quads is used to get the desired low-pass filter.

A decoder and a chain of transmission gates are used to design the analog multiplexer which facilitates the user to select the channel on which pre-processing has to be done.

II. DESIGN FLOW

2.1 Current Source Design

Current sources which supply current in the orders of milli-amperes consume huge on-die area. By using transistors working in saturation region and adjusting their sizes, any ratio of the supply current can be mirrored and steered from a single current source to the entire circuit. Using this concept, a current source of micro-amperes is employed through which hundreds of micro-amperes of required current is mirrored into each of the Op-Amps in the circuit. We are using a 100µA current source in our design.

2.2. Amplifier Design

Before starting the design of the amplifier, certain specifications are available at our disposal. These include V_{DD}, Tail current I_{SS}, Maximum Slew rate, Unity Gain Bandwidth (UGBW), Load Capacitance C_L, Maximum power to be drawn and output swing. For the set of transistors to work as an amplifier, each of them has to work in the saturation region. Hence the condition needed to be satisfied, in case of a

$$\text{NMOS is: } V_{ds} > V_{dsat} \text{ and PMOS is: } V_{sd} > |V_{dsat}| \qquad (1)$$

Initially, we assume certain V_{dsat} for each of the transistors. Further, we allocate a margin of twice the sum of the V_{dsat} of all the transistors and also allocate the amount of output swing. This margin voltage will be helpful in cases when there is a shifting of common-mode of the amplifier due to certain design approximations [2].

Hence, we can now formulate:

$$V_{dsatin} + V_{dsatload} = V_{DSAT} \qquad (2)$$

$$\text{Margin} = 2\, V_{DSAT} \qquad (3)$$

Hence,

$$V_{DSAT} + \text{Margin} + \text{Output Swing} = V_{DD} \qquad (4)$$

To make sure that all the transistors in the branch are in saturation, we allocate a certain V_{ds}, just like how we allocated V_{dsat} in the previous step, to each of the transistors. The condition to be satisfied here is,

$$V_{dsin} + V_{dsload} = V_{DD} \qquad (5)$$

In analog design, the finger width of each of the transistor is kept constant. This is to reduce gate resistance. Further, if we use a single finger instead of serially connected fingers, then the time for the current to travel from one end of

the finger to the other end is more. It is possible to calculate the trans-conductance of the input transistors, if the load capacitance and the UGBW are known. The relationship is as follows:

$$UGBW = g_{min} / (2 * \pi * C_L) \quad (6)$$

Further, with the given maximum power, P_{max}, it is possible to calculate the maximum amount of current that we can draw into the amplifier as,

$$P_{max} = V_{DD} * I_{SSmax} \quad (7)$$

For design purposes, it is possible to choose a convenient I_{SS} which is less than I_{SSmax}. Choosing a value too low will prompt us to use larger MOSFET's for the design, while choosing a value too large, say I_{SSmax}, we will be burning a large amount of power. Hence there exists a trade-off between area and power and it the decision of the designer which paves the way for further design. With the help of the calculated g_m, allocated V_{dsat}, allocated I_{SS} and the current to be burnt we can calculate the *W/L* of the input transistors. It is to be made sure that the length, *L* of these transistors is kept to minimum. This is because, the entire switching activity happens at this transistor and for the circuit to be fast, we need the *L* to be minimum, which for a 90nm technology is given as 100nm. The *L* for the load transistors is usually higher, in-order to obtain higher R_{out}, which ultimately will reflect on the gain of the amplifier.

It is needed for us to have a gain as high as 60dB and hence a telescopic single-stage amplifier, gain boosted using auxiliary NMOS and PMOS amplifiers has been designed. Implementing this in Cadence, a gain of 64.5dB has been obtained.

2.3 Common-Mode Feedback Design (CMFB)

Different topologies of CMFB are available for usage, and basing on the requirements of the user, the designer can choose [2]. The sizing strategy that is to be followed is as follows. The sizes of the four input transistors are equal, and are given by:

$$(W/L)_{in} = 1/\text{mirroring ratio} * (W/L)_1 \quad (8)$$

Where $(W/L)_1$ is the size of the input transistors of the amplifier. While, the sizes of the load transistors are given by,

$$(W/L)_{load} = 1/\text{mirroring ratio} * 2 * (W/L)_4 \quad (9)$$

Where $(W/L)_4$ is the size of the load transistor in the amplifier.

2.4 Differential Amplifier Second-Stage Design

The second-stage is usually a common-source amplifier. Also, if the first-stage is a PMOS based amplifier, then the second-stage is an NMOS based amplifier. Now, the second-stage of the Op-Amp introduces a new set of poles, in addition to the poles introduced by the first stage [3]. So, in-order for the system to be stable and to ensure that these poles do not interfere, we shift the poles of the second-stage further away from those of the first-stage by at least5 times. This can be achieved by burning 5 times of the current being burnt in the first stage. The sizes can then be calculated from the design steps as mentioned in the first stage. To obtain high swing of 600mV rail to rail, two stage amplifier has been designed which gives a gain of 82.34 dB.

2.5. Frequency Compensation

The phase margin to be achieved is 60 degrees, to ensure that the system is stable. Frequency compensation involves placing a resistance-capacitance pair in between the two stages of the Op-Amp. The values of the resistance and capacitance are varied using the parametric analysis of the Cadence tool and the phase margin is plotted. The values of resistance and capacitance for which the phase margin is 60 degrees, is taken as the compensation resistance-capacitance.

2.6 Bi-quad Design

The Ackerberg-Mossberg bi-quad is found to operate at relatively high frequencies even for large Q values [1]. Therefore we used an Ackerberg-Mossberg bi-quad in our design. The number of poles required toachieve the given

cut-off and roll-off is found to be eight. The transfer function of the filter is calculated using the cut-off frequency and the location of the poles. The transfer function is divided into four second-order transfer functions and each of the transfer functions is implemented using a different bi-quad. The capacitance and resistance values for each of the bi-quads are calculated separately according to the placement of the poles using the equation.

$$\omega_0 = 1/R*C \qquad (10)$$

where, ω_0 is the frequency of the pole location [1].

In order to minimize the area of the system, small capacitances (in the order of pico farads) are used.A gain of 35.56 dB has to be achieved. This is done by distributing the gain among the four bi-quads according to the value of Q. The first three bi-quads require only single stage Op-Amps and hence the single stage Op-Amp which we have designed earlier can be used. Since the output swing is also a major concern in our design, the last bi-quad requires a single stage Op-Amps and a two stage Op-Amps. All the bi-quads are connected in series and the output of the last bi-quad is taken as the final output of the filter.

2.7 128 Input Multiplexer

Initially the signal which is to be pre-processed i.e., filtered and amplified has to be selected. The selection is done by choosing one channel among the 128 channels available and the signal obtained through that channel is pre-processed. The signal inputs are directly given to a chain of transmission gates. These transmission gates are controlled by using a decoder. This whole system acts as a 128 multi-channel multiplexer which has the decoder inputs as the select lines. Thus the required channel on which the pre-processing has to be done is selected by manually controlling the decoder inputs. It is also possible to design a digital logic, based on the requirements of the user which can then perform automatic selection of the input.

III. SIMULATION RESULTS

The simulation results of our system are shown here. Fig.2 is the Cadence implementation of the differential Ackerberg-Mossberg bi-quad with two Op-Amps connected in inverting and non-inverting configurations. Fig.3 is the overall filter design as a cascade of four bi-quads. Fig.4 and 5 are the gain and phase plots of the overall filter and of each bi-quad respectively. Fig.6 is the transient response at each node of the filter when a 5mV rail to rail sinusoid of frequency 2.5 KHz is given as input.

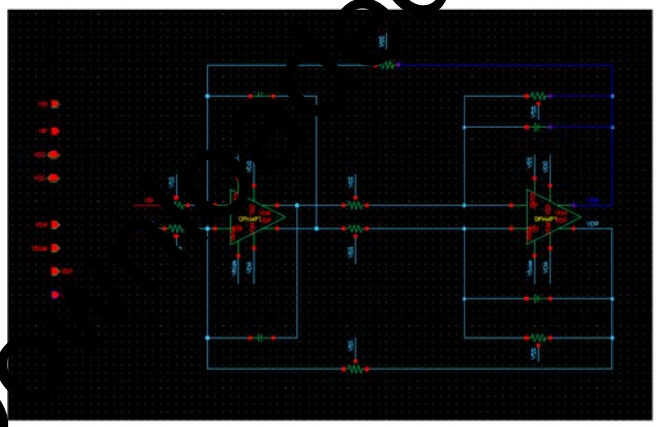

Fig.2. Bi-quad Design

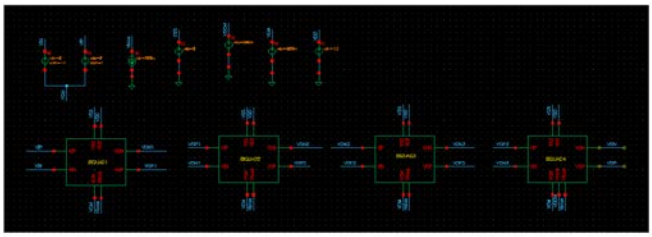

Fig.3. Overall Filter (Low-Pass) –Cascade of four Bi-quads

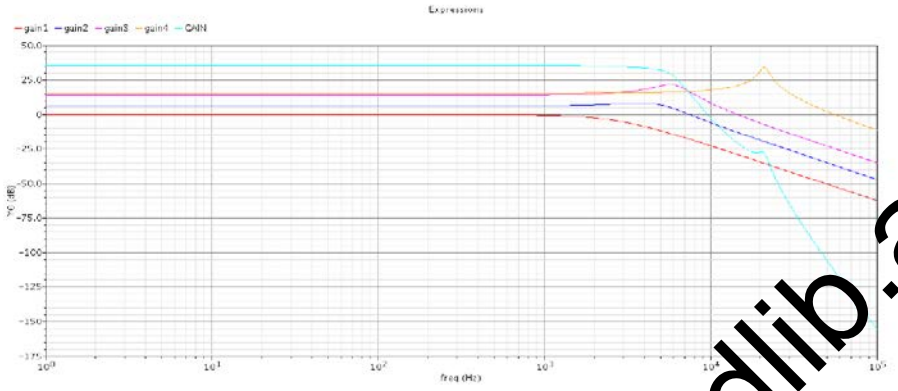

Fig.4. Gain Plot – Overall Filter and individual Bi-quads

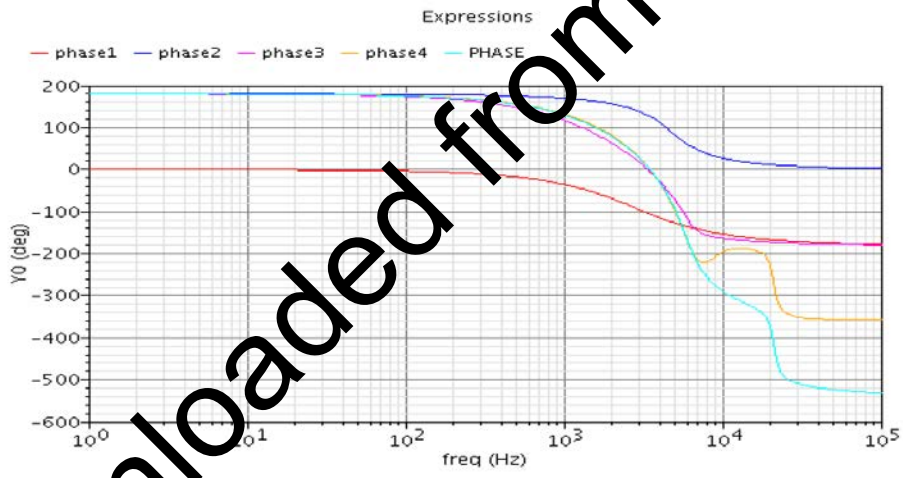

Fig.5. Phase Plot –Overall Filter and individual Bi-quads

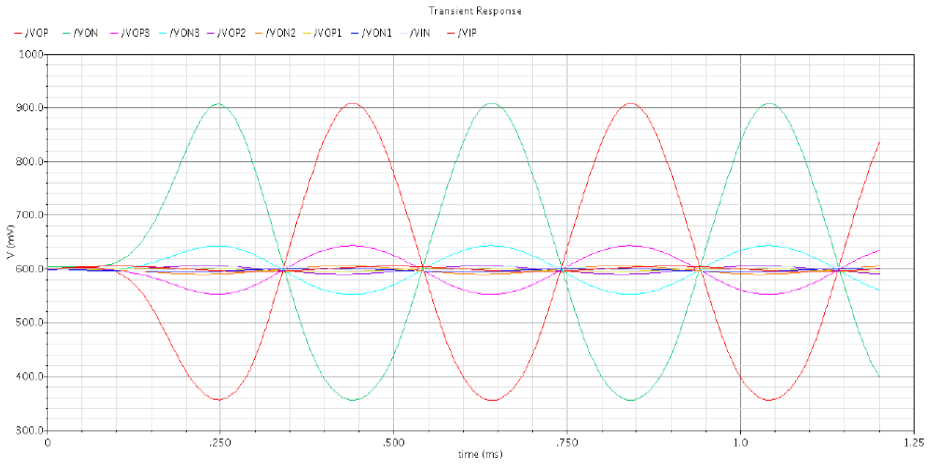

Fig.6. Transient Response at each node of the Filter

CONCLUSION

The eighth order low-pass filter which we have designed has a cut off of 4.80 KHz which is approximately equal to 5 KHz and a roll off of -140.56dB at 50 KHz. The Chebyshev implementation of Ackerberg-Mosseberg bi-quad provided better results when compared to Tow-Thomas Butterworth implementation and Sallen key bi-quad. The output common-mode of the designed operational amplifier is 600mV and the output swings obtained were from 300mV to 900mV which gives a rail to rail of 600mV as required. Unity Gain bandwidth of this Op-Amp is 700MHz. The overall filter has a gain of 35.56dB by obtained cascading four bi-quads each with a gain of 20.383mdB, 5.976dB, 13.995dB and 15.572dB respectively. The swings of the bi-quads are 7mV, 18mv, 91mV and 583mV respectively for 2.5 KHz input frequency. The area occupied by the system is approximately 0.4mm^2 and the power consumed is nearly 30mW.

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