Design and analysis VLSI Architectures using am bipolar MISFETs

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***Abstract*-Organic and inorganic thin film based transistor plays a major role in future generation electronic devices which uses micro, nano and picoelectronics circuits for inverters, oscillators, DRAM and backplane circuits in the display of most of the electronic devices with reduced power consumption. We analyzed based on self-assembled mono layer organic dielectric material Trichloro (Octadecyl) Silane (TOS) and a high- κ inorganic dielectric material Zirconium dioxide (ZrO2).Then we fabricated this Metal-Insulator-Semiconductor Field Effect Transistor (MISFET) with the configuration of Silver (Ag) as the metal at the top of the device as Source and Drain, pursued by the stack of TOS and ZrO2 as the Insulator (dielectric layer) which was previously coated on the ITO which act as the Semiconductor (Back Gate). Finally the IV characterization study illustrates the terrific result, which describes the am bipolarity operation, a future revolution in the unipolar n-channel and p-channel transistor.**

I. INTRODUCTION

Emergence of the metal-oxide-semiconductor (MOS) system over past 30 years witness the SiO2 gate oxide has been acting as the vital enabling material in scaling silicon MOS technology. As the gate oxide leakage is increasing with decreasing SiO2 thickness as well as SiO2 has reached atomic layer limitation level rejecting further reduction which makes repeated SiO2 gate oxide scaling is becoming extremely difficult. Since Moore's law extends scaling and device performance into the 21st century, for high-performance and low-power CMOS applications in the 45 nm nodes and beyond requires high-κ gate dielectrics and metal gate electrodes. Nevertheless, although the dielectric capacitance and strength of the gate dielectric are incredibly important properties the surface characteristics [1] of the gate dielectric can also plays a vital role. In addition to facilitating standard MOSFET, the high-κ dielectric/metal gate combination is also important for enabling future high performance and low gate leakage emerging thin film MOSFET built upon non-silicon high-mobility materials e.g. Ge, carbon nanotubes, and ITO substrates [13].

II. DESIGN METHODOLOGY

High dielectric-constant (k) gate dielectrics are characterized by a relatively rough surface morphology upon deposition in a vacuum chamber. The rough surfaces result in an inferior channel/dielectric interface along with poor Crystalline growth of the ODTS channel and thus OTFTs fabricated on such dielectric surfaces usually exhibit undesirable device characteristics with low current ON-OFF ratio. The rare earth oxides ($ZrO2$), $Er2O3$, $Pr2O3$, $ZrO2$ etc., are reported with very high dielectric constant and low leakage current reliable for gate dielectrics in microelectronics [9, 12]. ODTS film is deposited on $ZrO2$surface using two step deposition method. Deposited ODTS film is found poly crystalline in nature. ODTS organic semiconductors have become one of the most promising materials for future thin, light, and flexible display applications. The performance of the OTFTs can be improved by proper selection of Gate dielectric material and metal electrodes [11] (metals which can give well. In the normal OTFT's silicon is used but it consumes more power almost up to 20v so for reducing the power we are going for high-κ dielectric materials like ZrO2 which can reduce the voltage below 5v [4, 7].So the researchers all over the world are researching on various high dielectric constant insulators $Al2O3$ [7], $H\,fLaO$ [4,5],$H\,fSiOx$ [6], $Pr6O11$ [11], $La2O3$ [3] etc.

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III. EXPERIMENTAL DETAILS

This present work focuses on preparation of high quality Zirconium oxide (ZrO_2) thin films, a high-κ dielectric material by a modified sol-gel technique. The OTFT MIMFET transistor includes three layers such as the substrate layer or the metal layer, the oxide layer and the semiconductor layer.

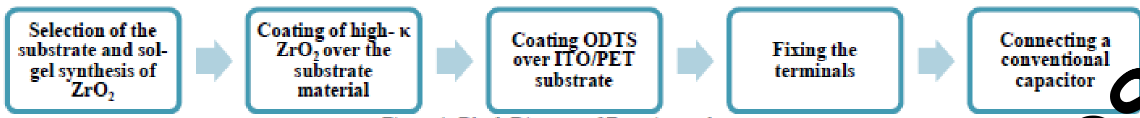

Figure 1. Block Diagram of Experimental setup.

The block diagram of experiment procedure is presented in fig.1. The experimental procedure for sol-gel Technique is to add Zirconium (IV) Prop oxide (2mL) in proper proportion with Iso Propyl Alcohol (9mL). Acetylacetone in Iso Propyl Alcohol was used as a gelatine agent. The prepared Zirconia is coated onto a glass plate and found that there was poor adhesion after firing ($100_{o}C$ for 5h). Hence a coating of Poly ethylene terephthalate (PET)was used before ZrO_2 film formation on a glass plate which results in better adhesive and uniform distribution. Since it is unable to peel off, the ZrO_2 film is coated on the flexible ITO /PET substrate. Then the commercially available ODTS is diluted by using Iso Propyl Alcohol and distilled water and its molecules are broken down to Nano size and are coated over the ZrO_2/PET layer. The terminals are soldered using the silver paste. Thus, the thin m MIMFET is fabricated using inorganic high-κ dielectric ZrO_2as the high-κ dielectrics and ODTS as the organic layer [1] on a flexible PET substrate as a self-assembled monolayer (SAM).

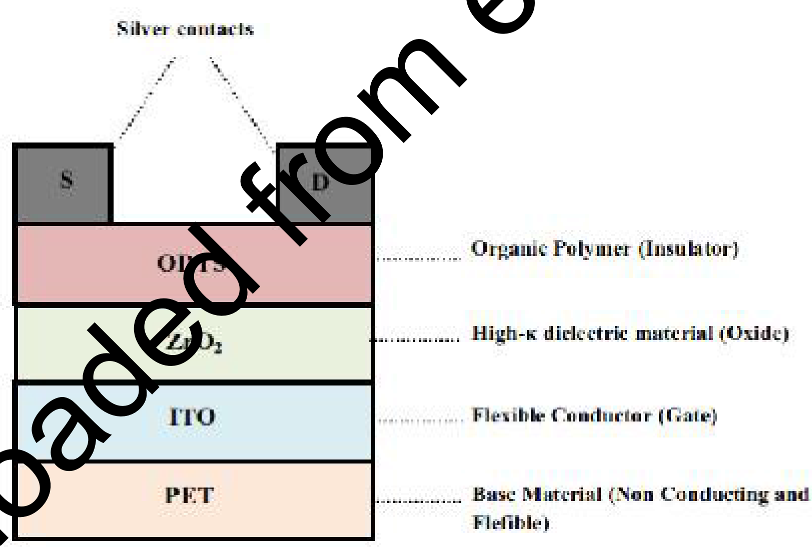

Figure 2. Structure of transistor.

Figure 3. Experimental arrangement of Layers

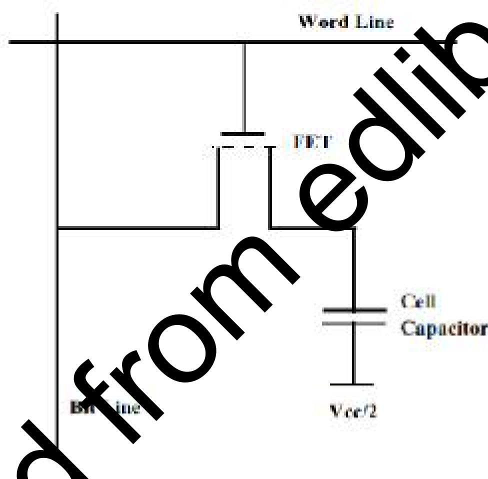

Figure 4. Structure of the DRAM.

Ultimately, the fabricated thin film OTFT MIMFET is connected with a conventional capacitor to form a DRAM cell and it is analyzed. The structure of DRAM cell with thin film OTFT is shown in the fig.4.

IV. RESULTS AND DISCUSSION

The fundamental principle of any FET is when a gate voltage is applied, as drain bias increases the current conduction between source and drain occurs. Figure 5 explores IV characteristics between the gate voltage (Vg) and the drain current (Id) at constant drain bias voltage (Vd) ranges from 0.05V to 2V.

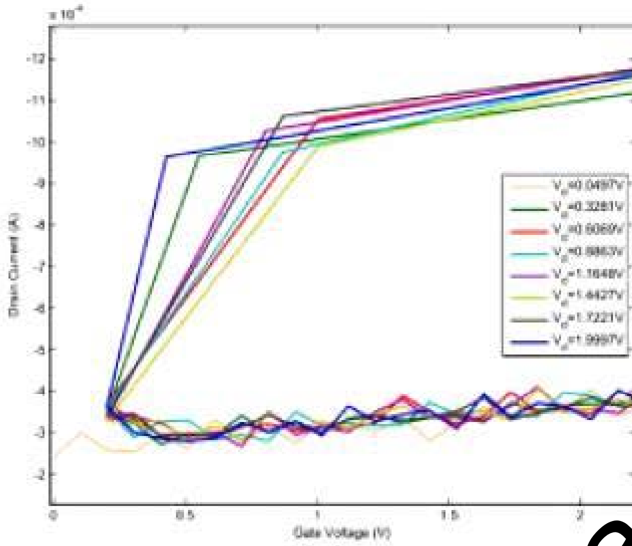

Figure 5. IV Characteristics of the stacked TFT.

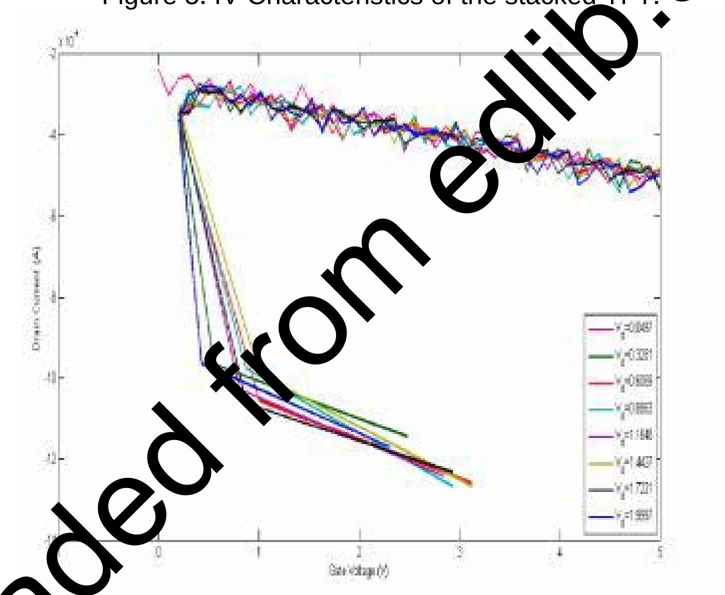

Figure 6. IV Characteristics.

The IV Characteristics gives following device nature. When positive voltage is applied the current conduction is from source to drain with the negative drain current. This describes the am bipolar nature of the carriers [3, 13]. When the device is active, it operates in the linear region between 0.3V to 1V and after that it starts to saturate. The threshold voltage is incredibly degraded to 0.3V. Therefore switching speed of the device is faster contrast to the traditionally used Si transistors.

V. SEM IMAGE

The SEM images of the prepared ODTS and Zirconia Nanoparticle are shown below.

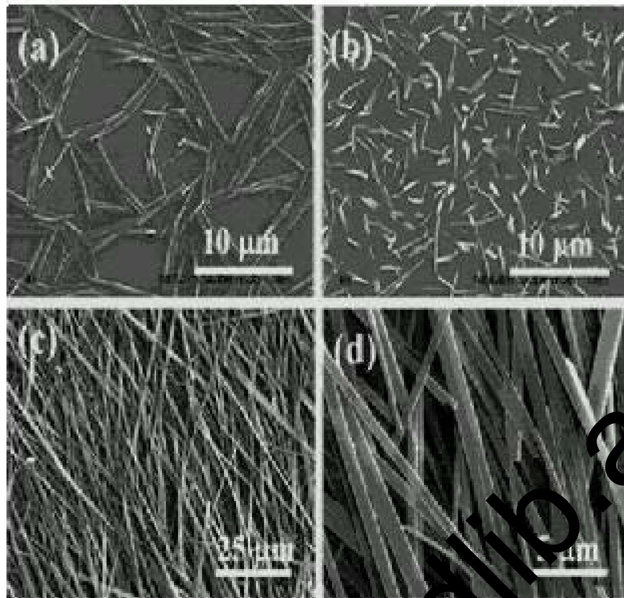

Figure 6. SEM image of ODTS.

The fig.7 displays SEM image of Zirconia in nano scale

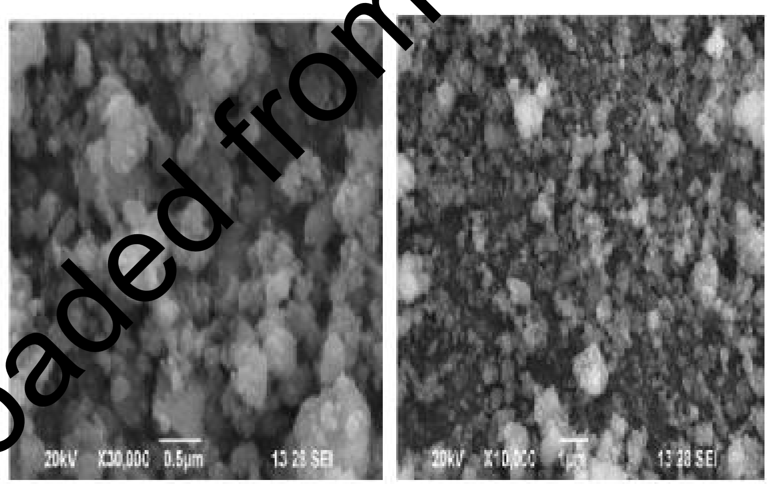

Figure 7. SEM image of Nano Zirconia.

CONCLUSION

The low voltage OTFTs are fabricated utilizing two step deposition on *ZrO2*dielectric. Since OTFTs possess low threshold voltage and sub threshold swing, they can be applied in portable devices. Numerous research works on low threshold voltage OTFTs have been presented but in those works complicated fabrication techniques sometimes more than one fabrication technique and insulating layers are employed. On the contrary, in this work we use traditional fabrication technique which is widely applied in commercial fabrications of TFTs, nowadays. Using this method, fabrication of low cost OTFT will become achievable so that the traditional Si-TFTs can be replaced.

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