Optimal Switching Strategy of Level shifted Carrier based PWM Technique for Asymmetric Multilevel Inverter

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Abstract- This paper present the optimal switching strategy for Asymmetric cascaded multilevel inverter (ACMLI) to drive a Brushless DC motor. Multicarrier strategy introduced for the multilevel inverters become more popular due to reduced cost, lower harmonic distortion & higher voltage capability as compared to conventional switching strategy applied to inverters. A new family of multilevel inverters with decreased number of separate DC sources has emerged named as ternary multilevel inverter. An assortment of topologies and modulation strategies has been reported for utility & drive applications. Phase Disposition modulation techniques are proposed to investigate the performance of asymmetric cascaded multilevel inverter. Feasibility of the proposed approach and the results are verified through Mat lab simulations and experimental results. Proposed modulation technique can easily be extended to three phase. A prototype of Asymmetric cascaded multilevel inverter is developed, using ARM® Cortex™-M0 Core (NUC140XXCN) controller to verify the theoretical and simulation results.

I. Introduction

Recently, Multilevel inverter finds applications mainly in industries such as Brushless DC motor, AC power supplies, renewable energy sources, drive systems, etc. The multilevel inverter has introduced the solution to increase the converter output voltage above the voltage limits of classical semiconductors. A new hybrid asymmetric multilevel inverter is introduced for 27 levels with minimum number of switches. This achieves a better sinusoidal output [1]. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [2]. An assortment of modulation strategies has been introduced for the cascaded multi-level inverters to reduce the harmonic contents further [3]. Of all the topologies Cascaded has many advantages than diode clamped and capacitor clamped inverter. Further studies on cascaded multilevel inverters were performed to highlight the advantage of cascaded multilevel inverter and the switching patterns are analysed. The concept of sinusoidal PWM modulation was introduced in an attempt to reduce the harmonic contents at the output voltage Level shifting is an emerging modulation and control technique. It gives better result compared with the phase shifting technique. Level shifting is done to reduce the harmonics at the output voltage. This paper investigates a control technique applied to the ternary asymmetric cascaded multi-level inverter to ensure an efficient voltage utilization and better harmonic spectrum.

II. Ternary Asymmetric Cascaded Multilevel Inverter

The structure introduced in this work is a ternary asymmetric cascaded multilevel inverter, which uses unequal DC Sources. The general function of this multilevel inverter is the same as that of the other two inverters. The multilevel inverter using Asymmetric cascaded-inverter provides a large number of output voltage levels without increasing the number of full bridge units. This configuration provides higher voltage at higher modulation frequency due to which the topology can be employed for high power applications. Due to the reduction in the number of DC sources employed, the structure becomes more reliable and the output voltage has higher resolution due to increased number of steps. This configuration recently becomes

very popular in AC power supply and adjustable speed drive applications. An asymmetric cascaded H-bridge inverter circuit is shown in Figure. 1.

In this proposed model ternary DC voltages progressions of unequal DC sources of ACMLI are used. This is most popular of unequal voltage progression with amplitude of DC voltage having ratio 1:3:9:27;81....3N and the maximum output voltage reach to ((3N-1)/2) V_{dc} . ACHB consist of 3-bridges is used to generate 27 level output for the DC Sources of 9:3:1 ratio. The output waveform 27 levels as ±13Vdc .....±1Vdc and zero. By different combinations of the 12 switches, S1-S12, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. Let the output of H bridge-1 is denoted as V_1 (t), the output of H bridge-2 is denoted as V_2(t) and H bridge-3 is denoted as V_3(t).Hence the output voltage is given by

$$V(t) = V_1(t) + V_2(t) + V_3(t) \quad (1)$$

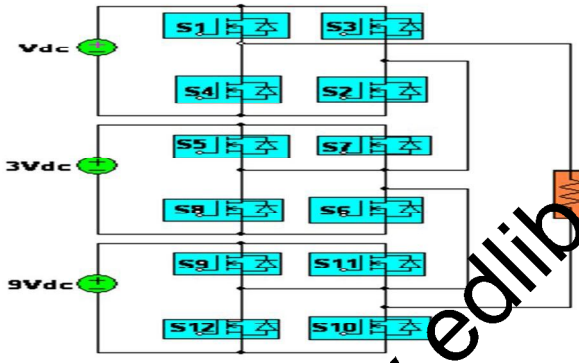


Figure. 1 Structure of 27 levels multilevel cascaded inverter

Table I: Switching states of proposed multilevel inverter during positive half cycle

Level	Output voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	V_{dc}	1	0	0	0	1	0	1	0	1	0	1	0
2	$2V_{dc}$	0	0	1	1	1	1	0	0	0	1	0	1
3	$3V_{dc}$	0	1	0	1	1	1	0	0	0	1	0	1
4	$4V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
5	$5V_{dc}$	0	0	1	1	0	0	1	1	1	1	0	0
6	$6V_{dc}$	0	1	0	1	0	0	1	1	1	1	0	0
7	$7V_{dc}$	1	1	0	0	0	0	1	1	1	1	0	0
8	$8V_{dc}$	0	0	1	1	0	1	0	1	1	1	0	0
9	$9V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
10	$10V_{dc}$	1	1	0	0	0	1	0	1	1	1	0	0
11	$11V_{dc}$	0	0	1	1	1	1	0	0	1	1	0	0
12	$12V_{dc}$	0	1	0	1	1	1	0	0	1	1	0	0
13	$13V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0

III. Iticarrier Based PWM Methods

Pulse Width Modulation refers to a method of carrying information on a train of pulses, the information is encoded in the width of each pulse. This technique helps in maintaining a constant voltage. In the carrier-based multilevel modulation, each level in a phase requires a carrier of its own. Carrier-based modulation schemes are mainly divided into two categories: level-shifted (LSPWM) and phase-

shifted (PSPWM) methods. Both of these have several variations, which differ by the allocation of module carriers with respect to each other [4]. In all level-shifted PWM methods, the carriers of the modules have a frequency of $f_{car} = 1/T_{SW}$ where the frequency of the carrier signal is inversely proportional to the switching period of the device (The range of the f_{car} is selected between 10 kHz to 100 kHz). The reference voltage, on the other hand, can have values of the range $-MV_{dc}$ and MV_{dc}. To cover the whole voltage range, the carriers are the triangular waves with same phase and peak to peak amplitude and arranged vertically, so that the carrier of the first module covers the range from zero to V_{dc}, while the second covers the range from V_{dc} to $2V_{dc}$. The last module covers the voltage from $(M-1)$ V_{dc} to MV_{dc}.This method is generally used in CMLI as it gives reduced THD [5]. Therefore, an inverter with *M*-modules in series is usually referred to as an *n*-level inverter and the number of levels can be calculated as given in Eq. (2).

$$n = 2M + 1 \quad \text{... (2)}$$

In the phase disposition (PD), all the carriers are in phase across all the bands. This gives rise to the lowest harmonic in the higher modulation indices, when compared to the other disposition methods. The level shifted multicarrier modulation offers better harmonic attenuation, but also offers an unequal device condition.

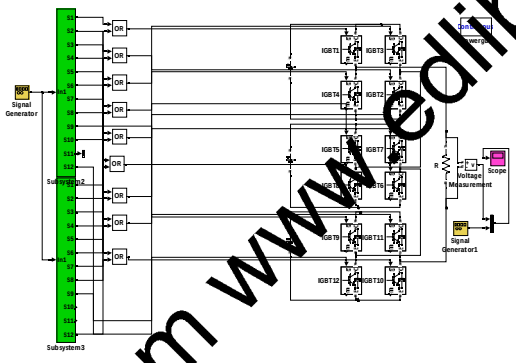


Figure.2. Simulink model of Asymmetric multicarrier PWM inverter

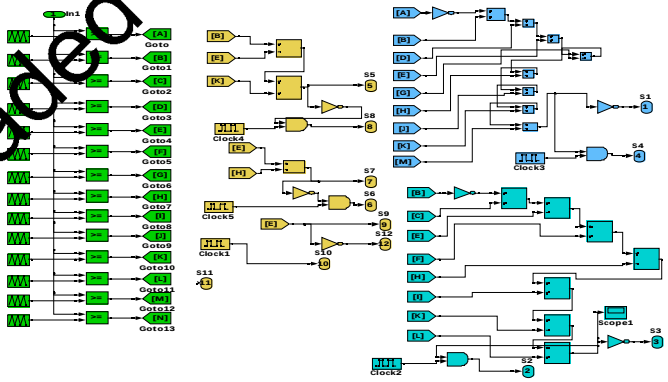


Figure .3 Subsystem - PD modulation for positive half cycle

IV. Results and Discussion

The feasibility of the proposed PWM strategy has been investigated and verified through simulation results, for both multilevel inverter and multi carrier PWM inverter, ternary asymmetric cascaded

multilevel inverter. The proposed technique for a twenty seven levels inverter with asymmetric DC sources involves the usage of only three DC cells. The voltages are given in the ratio of 9:3:1 with which a twenty seven level can be achieved with only three DC sources. The simulink model for an asymmetric multicarrier PWM MLI is shown in Fig. 2 they are created with a separate subsystem. The pulses are generated with the developed pattern and given to the corresponding switches via the subsystems. Higher the level , the harmonics are reduced to greater extent. To determine the harmonics in the proposed circuit, the FFT analysis is performed .Modulation technique is the logical extension of the sine triangle PWM multilevel inverter, in which n-1 carriers are needed for an n-level inverter. The preferred type is Phase disposition. The carriers are arranged in vertical shifts in continuous bands defined by the levels of the inverter. Each carrier has the same frequency and amplitude, the switching pattern and the carrier arrangements are shown in Fig.4 (a) .

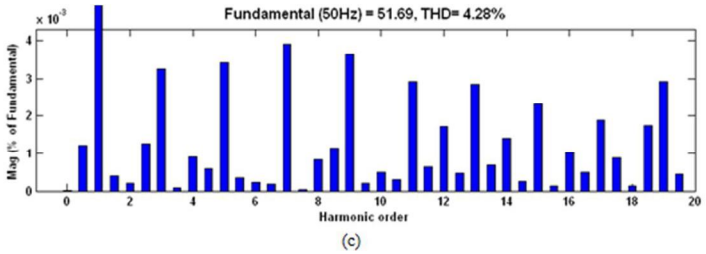
An n-level inverter using level shifted multicarrier modulation scheme requires (n-1) triangular carriers, all having same frequency and peak to peak amplitude, hence for 27-level inverter, 26 carriers are used. The modulated output for the PD multicarrier PWM 27 level multilevel inverter is shown in Fig. 4(b). Modulation is generally performed in any circuit to reduce the harmonic content at the output voltage. The harmonic content after modulation is analyzed by the FFT spectrum shown in Fig.4 (c). It is clear from the FFT analysis that the harmonics are reduced to a greater extent after modulation. To perform the other modulations with the same circuit the variations are only with the multicarrier that have been generated. The only difference is with the carriers that has been generated inside the subsystems for both positive and negative cycles. The main circuit model remains the same for the other two modulations. But only the subsystem varies with this. It is found that THD is considerably reduced after modulation is being performed. From the simulation work it is known that the PD technique produces lesser harmonic on a line-to-line basis compared to the other two techniques because it puts harmonic energy directly into a common mode carrier component which cancels across the line-to-line outputs.

To validate the proposed concept, the inverter is implemented and its prototype has been manufactured. The power supply circuit comprises of a step down transformer and a voltage regulator IC 7805 and 7812, which provides the DC voltage to the controller and the driver circuit. ARM® Cortex™-M0 Core NUC140XXCN microcontroller is used to provide the driving pulses because of its superior features like

I. Meeting the computing needs of the task on hand efficiently and cost effectively.
II. The NuMicro™ NUC100 Series is 32-bit microcontrollers with embedded ARM® Cortex™-M0 core the cost is equivalent to traditional 8-bit microcontroller
III. Wide availability and reliable sources

The control circuit decides the sequence of pulses to be given to the switches in the power circuit. The driver circuit amplifies the pulses to the required level. The driver circuit is used for an isolation of the negative current to the micro-controller, amplification of voltage and to create a constant voltage source. A power circuit is fabricated using 12 MOSFETs (IRF540), and it requires three individual DC sources of an asymmetric ternary ratio. As per the switching sequence presented in Table 1, the pulse signals generated by taking comparition and applied to the MOSFET switches, using the micro-controller. MOSFET with anti-parallel diodes are employed as switching devices. The opto coupler used for high side switch is 6N137, which is an optically coupled gate that combines a gallium-arsenide infrared-emitting diode and an integrated high gain photo detector. For low side switch MCT2E is used .Optocoupler circuit provides isolation between the control circuit and the power converter circuit. During the hardware implementation, the inverter is tested for 52V. Each inverter leg takes different voltages**.** During the implementation, the inverter input sources are taken as V_{dc1} = 4 V , V_{dc2} = 12V and V_{dc3} = 36V with switching frequency f = 50 Hz. As illustrated, the experimental setup is built for the generation of desired output voltage waveform. In order to reach the level, 3 unequal DC sources along with 12 switches are used. Fig. 5(a) and (b) depicts the experimental waveform of the inverter to generate driving pulses for the switches and the output voltage waveform of three bridges respectively. The output voltages with twenty seven-level stepped waveform can

be clearly appreciated; with low distortion. The hardware result obtained using arm processor is found to be in agreement with the simulation results.



(c)

Figure.4 (a) Switching pattern using PD carrier based scheme (b) Output Voltage waveform (c) Output voltage spectrum

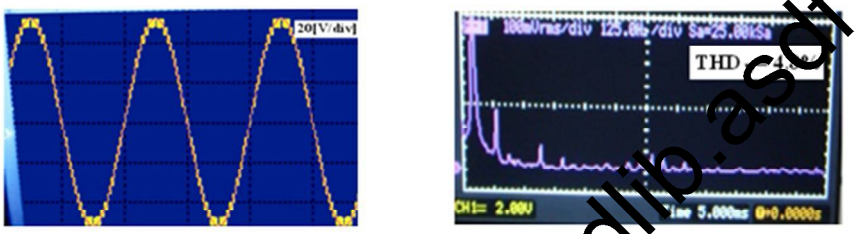


Fig.ure.5 .Experimental output voltage waveform and output voltage spectrum

V. conclusions

Optimal switching strategy of multicarrier PWM for Hybrid Asymmetric Multi Level Inverter has been presented. Simulink models for PD modulation are presented. The proposed strategy is so simple that it can be implemented even with few analog circuits. Also, the behavior of hybrid multi level inverter is presented with and without implementing Multicarrier strategy. Asymmetric MLI Topology uses reduced number of DC sources thus decreasing the complexity and the cost of the circuit. Moreover, this approach enables to obtain a twenty seven-level conversion with only three dc bus levels. This reduces the cost and offers the more number of levels at the output with a least number of primary devices and DC voltage sources. The results for both of the techniques are then compared against various performance indices. From the comparison, it is observed the THD obtained with MCPWM Inverter is comparatively lesser than the MLI. By increasing the number of steps, waveform approaches the desired sinusoidal shape and THD is reduced to IEEE standard. Proposed work can be extended to three phase and the same can be realized in hardware to drive high power motors such as PMBLDC motors and so on.

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