Electrical performance analysis of double gate transistor (DGMOS)

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Abstract—We present in this paper the main results of a two-dimensional numerical study based on the finite difference method. The static current-voltage characteristics I(V) of a double gate MOS transistor (DGMOS) are compared with a single gate MOSFET with SOI (Silicon On Insulate) technology. For this, we use a self consistent calculation of Schrodinger-Poisson coupled equations with pseudo-2D scheme. Simulation results show that the drain current values of the transistor DGMOS are higher compared with those of the SOI MOS transistor. In addition, the DIBL effect and the leakage current are minimized in the case of DGMOS. This confirms the performances of the double gate transistor and its ability to better control the channel and thus the drain current.

Keywords—single gate transistor MOSFET, double gate transistor DGMOS, Poisson equation, Schrödinger equation, DIBL, self consistent, leakage current.

I. INTRODUCTION

The semiconductor industry is always looking for developing semiconductor technology to finer geometries [1, 2].

The aim of the decrease in size of electronic devices is to reduce the cost and to improve the performances, but this, however, leads to the occurrence of adverse effects. To minimize these latter, it is interesting to turn to new transistor architectures such as double gate MOSFET which is now proving to be a very promising alternative [3, 4, 5].

II. STRUCTURE STUDIED

The schematic description of double-gate MOS device is shown in Fig. 1. It has 10 nm gate length \( L_G \), the gate oxide \( T_{ox} \) and Silicon body thicknesses \( T_{Si} \) are equal to 1.5 nm. The source and drain lengths \( L_{SD} \) are equal to 5 nm. The doping density is \( N_D = 10^{20} \text{cm}^{-3} \) in N+ source/drain regions and \( N_A =10^{10} \text{cm}^{-3} \) in the channel (P type). The work function of the gate material considered is 4.46 eV to achieve the theoretical threshold voltage \( V_T \) to 0.2V.

![Figure1. Schematic of double gate structure](image1)

We consider, in order to compare the electrical performances, a same transistor as the DGMOS structure (same size, same features) but a single gate one (Fig. 2).

![Figure2. Schematic of single gate structure with SOI technology](image2)

III. FUNDAMENTAL EQUATIONS

The size reduction devices to nanometric sizes reveal quantum phenomena, previously considered largely non-existent or negligible. For this, it is necessary to use equations derived from quantum mechanics [6]. The most rigorous approach is to solve the Poisson and Schrödinger equations simultaneously to take into account the quantum phenomena.
\[
\frac{d^2V(x,y)}{dx^2} + \frac{d^2V(x,y)}{dy^2} = \frac{\rho(x,y)}{\varepsilon_0 \varepsilon_r}, \tag{1}
\]
\[
\frac{\hbar^2}{2m} \frac{d^2\psi(y)}{dy^2} + qV(y)\psi(y) = E\psi(y) \tag{2}
\]

Where: \(\psi(y)\) is the wave function corresponding to the eigenvalue \(E\); \(V(y)\): the electrostatic potential and \(\rho(x)\) is the charge density.

We clearly see that the equations (1) and (2) are coupled. It is therefore self-consistency in their resolution [7, 8, 9]. We can illustrate the self-consistent system by the following one:

\[
\begin{align*}
\rho(y) &= S[V(y)] \\
V(y) &= P[\rho(y)]
\end{align*}
\]

Where: the functions \(S[V(y)]\) and \(P[\rho(y)]\) represent the Schrödinger and Poisson equations.

IV. Validation Model

In order to validate the obtained results, we compare our model with Sentaurus numerical simulation (ISE-TCAD software).

The comparison between the modelled and simulated characteristics gives good agreement for \(V_{GS}\) down to 0.4 V; these devices are operated at \(V_{GS}\) lower than 0.4 V (linear regime), and therefore, the model is valid for the regimes of practical interest.

![Figure 3](image1.png)

**Figure 3.** \(I_D\) vs. \(V_{DS}\) for a gate voltage of 0.6 V and thickness silicon of 2 nm

![Figure 4](image2.png)

**Figure 4.** \(I_D\) vs. \(V_{DS}\) for a gate voltage of 0.6 V and thickness silicon of 1.5 nm

The On-current \(I_{ON}\) (saturation current) is more important in the DGMOS compared with single gate transistor. Worth 2150 \(\mu A\) is for SOI MOS transistor and 2745 \(\mu A\) for DGMOS in the case of thickness silicon \(T_{si}=2\) nm.

On the transfer characteristic \(I_D(V_{GS})\) (fig. 5 and 6) we confirm the previous result \([I_{ON} (DGMOS)>I_{ON} (SOI)]\).
The Off-current \( I_{OFF} \) is significantly lower in the DGMOS than in the single gate. We can have a better control of the output current by considering DGMOS.

Fig. 9 shows the evolution of the conduction band in the DGMOS device \((V_{GS}=0V)\) for different drain voltage \( V_{DS}=10mV, 0.2V \) and \(0.6V\) with \(L_G=10nm\) and \(T_{Si}=1.5nm\). Is clearly shown the Drain Induced Barrier Lowering (DIBL).

Fig. 10.a and 10.b clearly illustrate that the DIBL effect is lower in DGMOS architecture.
In this section and the previous one, a comparison was achieved between a single gate and double gate transistor, to highlight that the transistor DGMOS gives better control of the channel compared to the single gate when decreases the thickness $T_{Si}$. This is summarized in the following table:

<table>
<thead>
<tr>
<th>Thickness $T_{Si}$ (nm)</th>
<th>$T_{Si}$=1.5nm</th>
<th>$T_{Si}$=2nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architectures SOI DGMOS</td>
<td>SOI DGMOS</td>
<td>SOI DGMOS</td>
</tr>
<tr>
<td>Saturation Current (I_{ON}) (µA)</td>
<td>1485</td>
<td>2150</td>
</tr>
<tr>
<td>Leakage Current (I_{OFF}) (µA)</td>
<td>0.94</td>
<td>27.37</td>
</tr>
<tr>
<td>Subthreshold slope (S) (mV/dec)</td>
<td>97</td>
<td>158</td>
</tr>
<tr>
<td>DIBL Effect (mV/V)</td>
<td>178</td>
<td>51</td>
</tr>
</tbody>
</table>