Performance of 15 nm Gate Length $In_{0.17}Al_{0.83}N$/GaN HEMT Used Simulation SILVACO Software.

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Abstract--We have simulated HEMT 15 nm length gate with ability in analysis DC, AC, Transit and high frequency characteristics. This work is the demonstration of motivation for HEMT with InAlN/GaN structure in different characteristics. The simulated HEMT devices with length gate 15 nm and materials InAlN show very good scalability. We have excellent exhibit g_m=0.85S/µm, I_{DSS}=0.59A/µm, V_{BR}=120V. The L_G = 15 nm devices also feature record high-frequency characteristics for HEMT design with f_T = 875 GHz and f_{Max} =1.1THz. More significantly, the periphery oxide of the Gate suppresses leakage current when compared with equivalent normal HEMTs.

Keywords: HEMT, 15nm length gate, Silvaco, InAlN/GaN.

I. Introduction

The HEMT has demonstrated to be an excellent model system to study fundamental physics and technology for devices issues and to provide well calibrated and relatively parasitic-free device results to support the development of simulators that would allows us to chart the future of this technology. And $In_{0.17}Al_{0.83}N$ is new material used today for potential successor AlGaN used takes advantage of the interesting material properties of the III-nitrides, such as a wide band gap (4.78eV), high breakdown electric field and excellent thermal conductivity, Interface of conduction is as of and the polarization charge causes its carrier concentration become larger than other HEMTs with different materials. Carrier concentration and thermal conductivity of the substrate is mainly responsible for power performance of a device at particular frequency band. Lattice constant of GaN is higher than AlN thus it provides better thermal response because it minimizes lattice mismatch better than AlN between the corresponding buffer layer and substrate. With the rapid progress and maturation over the last several years, wide band gap GaN-based high electron mobility transistors (HEMTs) are now widely regarded as the next generation technology leader for high frequency and high power device applications.

GaN based HEMTs have high breakdown voltage and don't need protection circuit [1]. The first HEMTs were developed mostly for low noise applications like receivers [3, 4, and 5].

The principal source of noise added by the transistor at high frequencies is related to power dissipation in the resistances of the device. At lower frequencies generation/recombination processes become dominant. General dependencies of F_{Min} on device parameters can be obtained from Fukui's the equation. Fukui showed that:

$$F_{Min} = 1 + 2\sqrt{K_G}\left(\frac{2\pi f C_{GS}}{g_m}\right)\sqrt{g_m\,(R_S + R_G)} \quad (1)$$

The InAlN-GaN heterostructure system enables high voltage, high current operation, resulting in the demonstration of >10X power performance than other material like GaAs or Silicon technologies.

The high RF power density (W/mm) directly translates into high watts per unit capacitance (W/pF), resulting in high impedance and simpler matching, an enabler for wide-bandwidth applications.

In this these, we will studied the DC, AC operation of InAlN/GaN HEMTs on substrates SiC [6]. An investigation of the influence of the new device model developed with nucleation and buffer layer on the power performance of InAlN/GaN HEMTs is conducted in the study. Also studies of GaN-based transistors for higher power at higher frequencies are done in the work. To achieve high performance, graded InAlN layer is used in device modeling.

Use of AlN or GaN cap layer has been proven to be effective in confining electrons in the channel and minimize short channel effect for high speed applications. By the use the periphery oxide Al_2O_3 of the Gate suppresses leakage current of the gate, the dislocation scattering mechanism & the electron spillover into the bulk are reduced and the 2DEG confinement is improved. In the subsequent study the material and model parameters for GaN and InAlN are discussed. They are incorporated in the two dimensional device simulators TCAD-Silvaco. The simulator is then calibrated against measurement data of a gate length, L_G= 15 nm modeled device at standard condition using the set of models and parameters predictive simulations. Good agreement for the DC, AC and Transit characteristics is achieved.

In this regard, there is great value in continuing to push the HEMTs technology so as to explore significant in the physics issues in the relevant dimensional range. Reduction of insulator thickness results in greatly increased gate leakage current [2].

This is what currently limits the reduction in HEMT lateral dimensions. Suppressing this, would allow us to scale the HEMT below 15 nm while preserving excellent RF characteristics. In this work, we demonstrated an the periphery oxide of the Gate HEMT design that mitigates forward gate leakage current by over two orders of magnitude and yields excellent characteristics.

II. Process Technology

Fig. 1 shows a cross section of epitaxial layer structure used in this work and a schematic of the simulated device structure. Our device features an InAlN/GaN heterostructure design where the periphery oxide Al_2O_3 of the Gate is a different with conventional designs. As a result, after a triple recess process [2], the doping layer is eliminated in the intrinsic device resulting in a doping-free InAlN barrier. This gives rise to a conduction band shape for the barrier that, for the same sheet carrier concentration.

Table 1: Parameter used for simulation in HEMT.

Name	Symbol	Value	Unit
Buffer	E_N	150	nm
Channel	E_{Ch}	38	nm
Barrier	E_D	12	nm

A. DC Characteristics of HEMT

Fig. 2 shows output characteristics of an HEMT with L_G of 15 nm. The device exhibits excellent pinch-off and saturation characteristics.

Fig. 3 shows output characteristics of an HEMT with L_G of 15 nm with Kink effect for temperature ambient. The device exhibits the variation of gate current with drain voltage shows a rise after stress but without abrupt growth in gate current at V_{DS}, kink. Both drain and gate currents recover to the fresh state, indicating no creation of traps. There- fore, the enhancement of the kink effect is probably due to the traps activated in the InAlN barrier layer.

Fig. 4 shows the transconductance and the Input characteristics of a 15 nm HEMT of a previously demonstrated normal $In_{0.17}Al_{0.83}N$ HEMT with a similar channel design, barrier thickness gate length, and other parameter in Table 1.

The HEMT displays comparable subthreshold characteristics to the normal HEMT with a subthreshold swing of V_T=-0.74V and g_m of 0.75 S/µm at V_{DS} = 2V.

B. AC Characteristics of HEMT

Fig. 5 shows Gain current H_{21} of HEMT with L_G of 15 nm. The device exhibits excellent characteristics at low results in frequency to 880GHz.

Fig. 6 shows Max Gain Power of HEMT with L_G of 15 nm. The device exhibits excellent characteristics at low results in frequency to 1.1THz.

Fig. 7 shows Unilateral Gain Power of HEMT with L_G of 15 nm. The device exhibits excellent characteristics at low results in frequency to 1.16THz.

Fig. 8 shows in and out Power of HEMT with L_G of 15 nm. The device exhibits excellent characteristics at out power results in frequency to 1.16THz.

Fig. 9 shows the on gain measurement result of a 40dB wide device when tuned for power. A power out of 3.5 W/mm was achieved along with 42 dB power gain. This increased power density was obtained at a reduced power out of 3.5 W, which is attributed to reduction of trapping effect due to improved epi quality and surface passivation. Since the trapping effect deteriorates with increased electric field or bias voltage for a specific device dimension, performance of the devices as a function of bias voltage can be used as a valid measure of this phenomenon.

Fig. 10 shows the measurement results of the InAlN/GaN HEMTs under a wide voltage bias range from 0 V to 20 V for V_{DS} and 0V to -5 V for V_{GS}, where the tuning was for optimum efficiency. It is seen that a relatively flat PAE plateau of 35-39% was achieved throughout the wide voltage span, illustrating flexibility of power-supply requirement for various applications. Simultaneously high power density of 3.5 W/mm and PAE of 39 % were obtained at 20V bias. The ability to achieve a high PAE at such a high bias voltage confirms the reduction of trapping effect with these devices. Obtaining a high PAE simultaneously with high power is essential for system insertion since dealing with the heat generated in inefficient amplifiers.

C. Transit Characteristics of HEMT

Fig. 11 shows Drain Lag of HEMT with L_G of 15 nm. The device exhibits excellent characteristics at the calculation of the drain obtained by simulation is 25%, we can say, however, that after analyzing the current delay is more pronounced when the trailing edge of the pulse drain the establishment of the drain current at high and low field.

Fig. 12 shows Gate Lag of HEMT with L_G of 15 nm. The device exhibits excellent characteristics at the calculation of the drain obtained by simulation is 26%.

This effect has its origin at the interface buffer / active layer HEMT; the electrons are injected into the buffer layer, where they are captured by the trap layer.

III. CONCLUSION

We have presented the power performance of 15 nm gate-length InAlN/GaN HEMTs on SiC substrates using the periphery oxide of the Gate. These devices exhibited current density as high as 0.59A/µm, Peak extrinsic transconductance of 0.85S/µm.

These results demonstrate the possibility of using this technology; we have presented an alternative explanation to the physical characteristics of the current pulses InAlN/GaN HEMT.

Resulting from structure InAlN/GaN of HEMT. The cover layer in addition to the drain and source with a Schottky layer analysis indicates that delay the speed of the simulation is to optimize atlas design to help the base property optimized.

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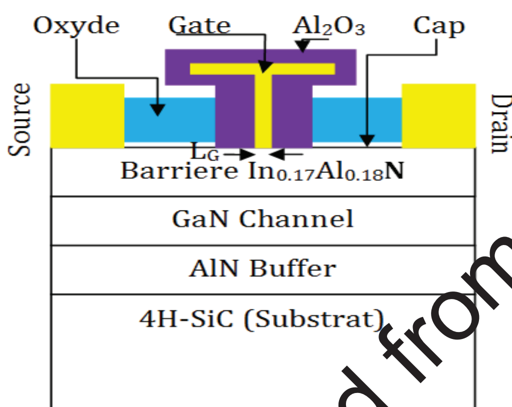

Figure 1. Heterostructure and schematic simulation of InAlN HEMT.

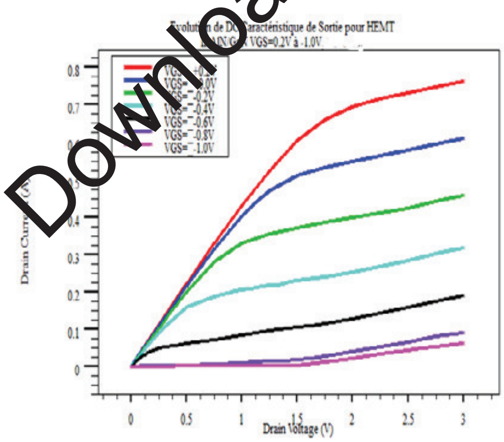

Figure 2. Output characteristics of 15 nm InAlN/GaN HEMT.

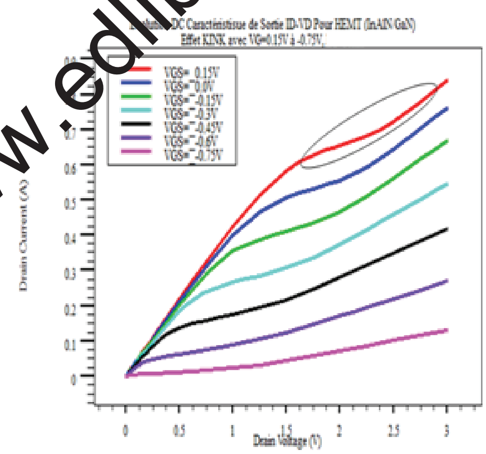

Figure 3. Output characteristics of 15 nm InAlN/GaN HEMT with Kink effect.

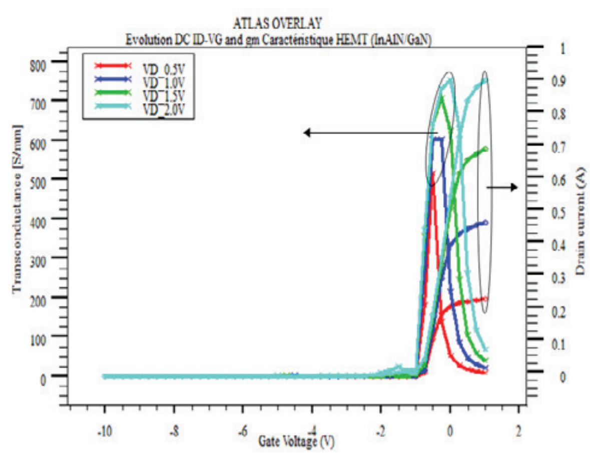

Figure 4. Transconductance and Input characteristics of 15 nm InAlN/GaN HEMT.

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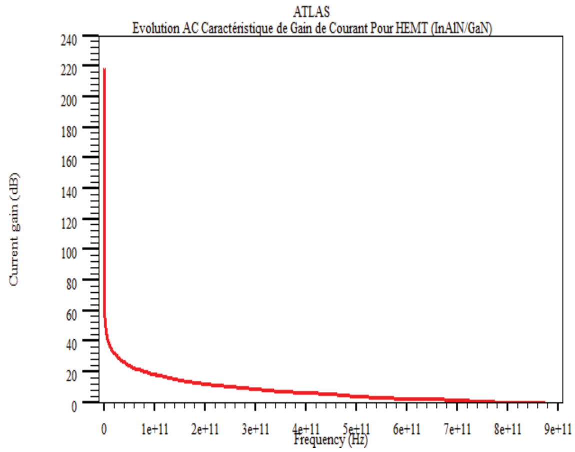

Figure 5. Gain current H_{21} of 15 nm InAlN/GaN HEMT with Temperature T=300K and V_{DS}=2V.

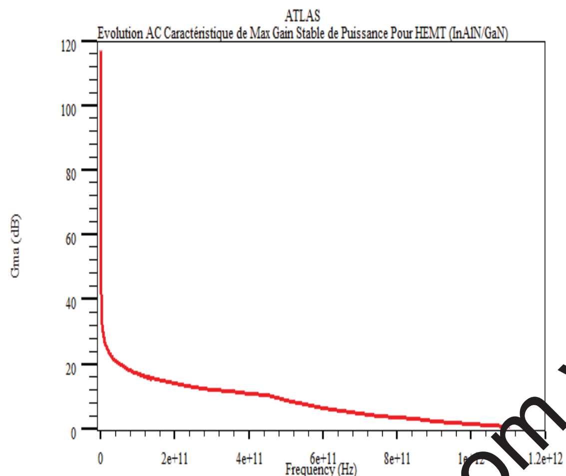

Figure 6. Max Gain stable Power of 15 nm InAlN/GaN HEMT with Temperature T=300K and V_{DS}=2V.

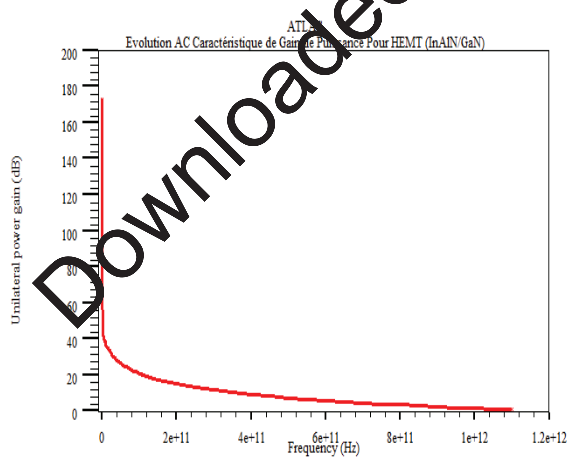

Figure 7. Unilateral Gain stable Power of 15 nm InAlN/GaN HEMT with TemperatureT=300K and V_{DS}=2V.

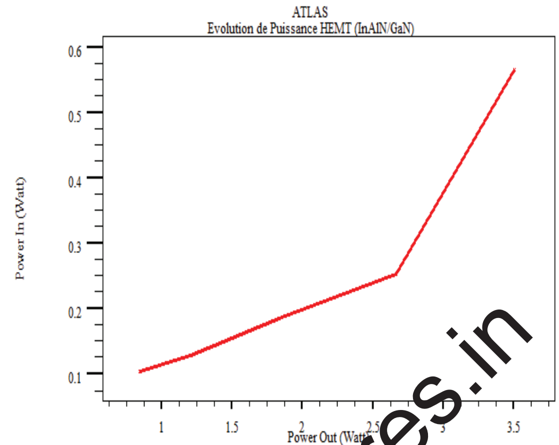

Figure 8. In and Out Power of 15 nm InAlN/GaN HEMT.

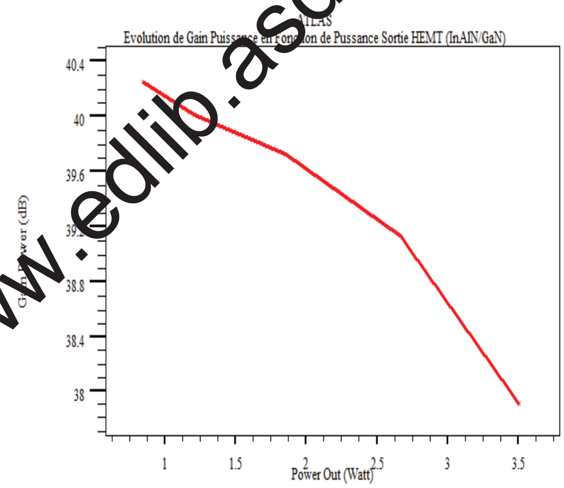

Figure 9. Power Gain of 15 nm InAlN/GaN HEMT.

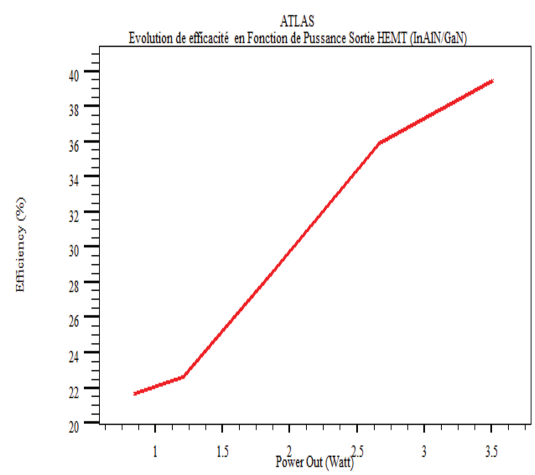

Figure 10. Efficiency of 15 nm InAlN/GaN HEMT.

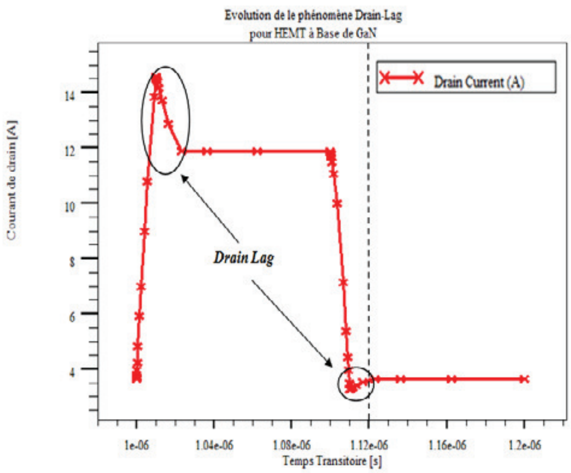

Figure 11. Drain Lag of 15 nm InAlN/GaN HEMT with Temperature T=300k, V_{GS}=0V and V_{DS}=20V.

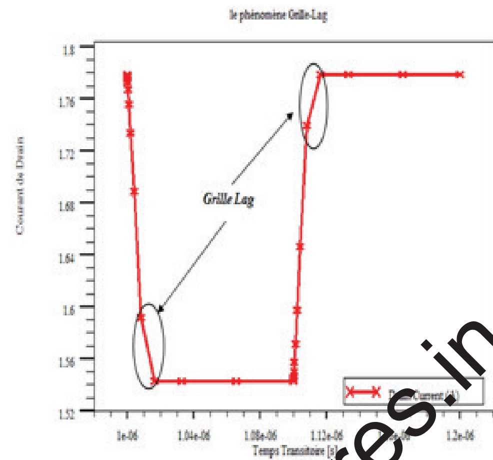

Figure 12. Gate Lag of 15 nm InAlN/GaN HEMT with Temperature T=300k, V_{GS}=-5V and V_{DS}=20V.