Characteristics sensitivity of DG SOI n-MOSFET to its Parameters variations

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Abstract—**The predictable decrease of transistors sizes which is nowadays close to the atomistic dimension leads today to nanometer devices. Double gate MOSFETs called DG MOSFETs are considered to be one of the most promising candidates for nanoscale CMOS devises. DG MOSFET might be the best viable alternative to build nano -MOSFETs when L_g < 50nm and it is well known that, in practice gate length in bulk MOSFETs are scaled to below 50 nm and gate lengths of experimental FETs [1] -[2] have approached currently 15 nm. DG MOSFETs demonstrated a perfect electrostatic control, a better control of the gate region with a reduction of short channel effects and a greater scalability. Transistors design parameters strongly affect the drain current. Our contribution in this paper allows highlighting the electrical characteristics sensitivity of the DG SOI n -MOSFETs to this device parameters variation. Simulation results we obtained in this study have been performed using SILVACO software [3].**

Keywords- double-gate MOSFETs; silvaco software; numerical simulation.

I. INTRODUCTION

All Silicon CMOS technology has emerged over the 25 years as the main technology of microelectronics industry for two unmistakable reasons: the first one is the rich supply of silicon wafers; and the second one is that a good oxide can be readily grown on silicon and this isn't achievable on germanium or else on some other semiconductors. Si-CMOS technology evolution is governed in industry by a trend knows as Moore's law, which states that transistors number on a chip doubles every 18 months. This trend has set such a point of reference that industry unofficially sets it as a target to be met in their product plans. In CMOS technology, MOSFET transistors scaling continuity has enabled IC's with lower power dissipation, higher speed and higher packing density. All these properties have been key components leading today's communication systems, computers, ects. The basic idea of MOSFET scaling is the progressive reduction of all its dimensions such as its length, width, gate oxide thickness, and also a reduction of doping density, with scaling of supply voltage in order to maintain a constant electric field throughout the device. All these reductions lead to a higher packing density, higher switching speed and lower power dissipation of IC's. However, as the MOSFET transistors dimensions scaled to the nanometer regime, several physical barriers became aspirant for future applications. Thus modifications to CMOS device structure to get better performances are required. In Sub-100 nm scale, MOSFET undergo rapid and fundamental architectural changes, which include double gate MOSFET transistors that have many advantages over traditional bulk MOSFETs. Double Gate (DG) MOSFETs seem to be a very promising option for ultimate scaling of CMOS technology because of their short channel effects immunity, reduced leakage current and more scaling potential. Due to their inherent performances advantages, DG MOSFET out-performs conventional single gate MOSFETs. DC analysis of DG devices has revealed that DG MOSFETs drain current and transconductance are equal to twice that of the drain current and transconductance of a single gate SOI MOSFET [4, 5, 6] with the same dimensions, and this is mainly due to volume inversion phenomena. In this work, we attempt to focus on numerical simulation of a double-gate n-MOSFET in order to highlight its parameters variations effects on its drain current.

II. SIMULATED DEVICE

Several different DG-MOSFETs structures have been proposed to deal with fabrication issues, including planar and quasi-planar structures. DG-MOSFETs fabrication is complicated, and the alignment of top and bottom gates is hard to reach, but this alignment is crucial for good device performance. Misaligned gates result in extra capacitance and also result in loss of current drive. In this work we consider an ideal symmetrical planar DG MOSFET where its two channels facing each-other are activated simultaneously and feature identical charge and mobility. A Schematic diagram of a DG MOSFET is shown in Fig. 1. In Fig. 2 is shown a Double gate MOSFET under Scanning Electron Microscopy.

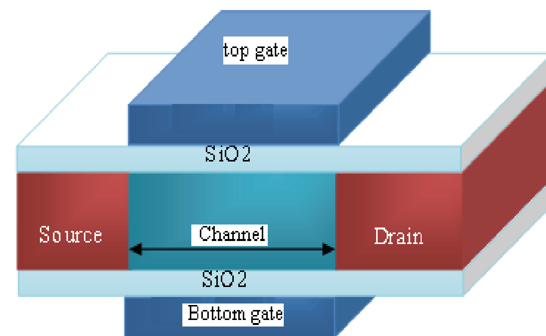

Figure 1. A Schematic diagram of a Double Gate MOSFET.

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Figure 2. DG MOSFET structure under Scanning Electron Microscopy [7].

In Double gate MOSFETs, gate voltage controls the electric field determining the amount of current flow through the channel. The most common mode of operation is to switch both gates concurrently, and this is the mode used in this work.

Device simulation is applied to evaluate the electrical behavior of our device. The information about the device geometry and the local doping concentrations must be given by some kind of solid modeling or full process simulation.

The standard model for universal devices simulations is the semi-classical transport simulation of electrons and holes based on the drift diffusion approximation called DD model. The conduction in this model is governed by a set of five fundamental, partial-differential equations which are: Poisson equation, continuity equations for holes and electrons; equations for hole and electron densities that are solved to describe the carrier, current and field distribution in the device. A numerical solution requires a discretization of the simulation region; this means the equations are solved on specific points on a grid. On these grid points the doping information must be given and the electrical contacts of the device must be defined as boundary conditions of the region borders.

Poisson equation (1) and carrier's continuity equations (2) and (3) are given by [3], [8], [9]:

Poisson equation

$$\nabla^2 V = -\frac{q}{\varepsilon}(p - n + N_D^+ - N_A^-). \tag{1}$$

Electron current continuity equation

$$\frac{\partial n}{\partial t} = -\frac{\nabla \overrightarrow{J_n}}{q} + G - R . \tag{2}$$

Hole current continuity equation

$$\frac{\partial p}{\partial t} = -\frac{\nabla \overrightarrow{J_p}}{q} + G - R . \tag{3}$$

Electron current equation

$$\overrightarrow{J_n} = q.n.\mu_n.\vec{E} + q.D_n.\overrightarrow{\nabla_n} . \tag{4}$$

Hole current equation

$$\overrightarrow{J_n} = q.p.\mu_p.\vec{E} - q.D_p.\overrightarrow{\nabla_p} . \tag{5}$$

Where: q is the elementary charge (As); ε is the semiconductor permittivity (As/Vm); p and n are hole and electron density (cm^{-3}); N_D^+ and N_A^- are correspondingly ionized donor and acceptor density concentration (cm^{-3}), R and G are recombination and generation rate ($cm^{-3}s^{-1}$) ***J***n and ***J***p, are current densities (A/cm^2); D_n and D_p are diffusion coefficients (cm^2s^{-1}), μ_n and μ_p are respectively electrons and holes motilities (cm^2/Vs).

In this work, device simulation tool ATLAS (SILVACO) is used to simulate the electric properties of a 2 dimensional designed DGFET standard structure represented in Fig.3. Atlas widely used semiconductor companies, allows performing physically-based 2D/3D device simulations permitting predicting the electrical behavior of specified semiconductor structures and provides insight into the internal physical mechanisms associated with the device operation.

Within the calculator, the fundamental equations used are based on the usual drift-diffusion model of charge transport with Fermi-Dirac statistics. The equations Solutions are achieved by Gummel algorithm. All the models used (models for low field mobility, model for velocity saturation) are implemented in ATLAS SILVACO software.

III. SIMULATION RESULTS

The starting point for our simulations is the basic structure of a symmetrical DG n-MOSFET represented in Fig.3. The different parameters of our structure are assumed as follows:

Channel doping $N_A = 10^{18}/cm^3$; source/drain doping $N_D = 10^{20}/cm^3$; Drain and source length $L_{GS}=L_{GD}=3nm$; silicon film thickness $t_{si}=3nm$; gate length $L_G=24nm$.

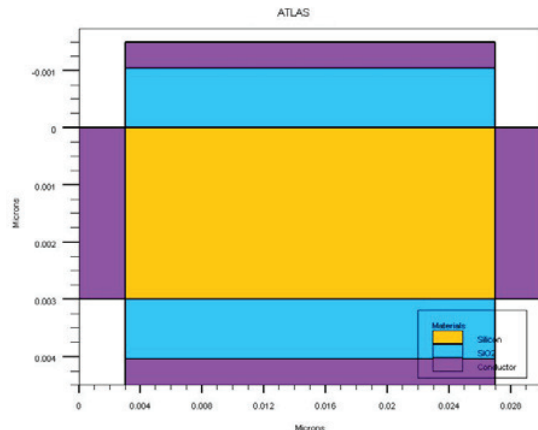

Figure 3. ATLAS simulation of the DG MOSFET considered.

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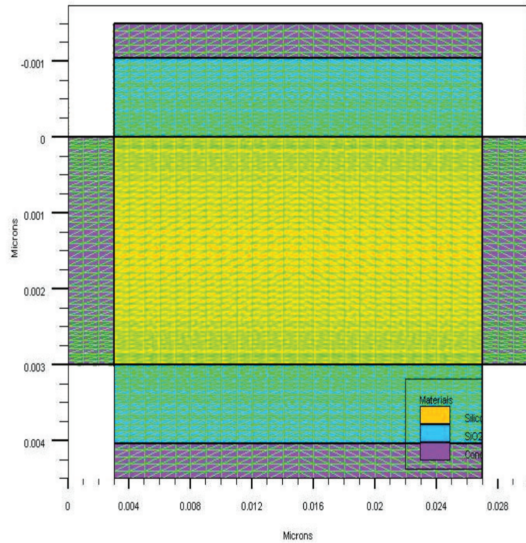

Figure 4 Mesh on the planar DG n-MOSFET structure.

Mesh parameters are adjusted to create desired mesh as we did in Fig 4.

It is well known that mesh condition affects the electron flow inside the device. In our DGFET finer mesh is applied at Si/SiO_2 interfaces.

Figs 5 and 6 present output and transfer characteristics of the conceived double gate transistor.

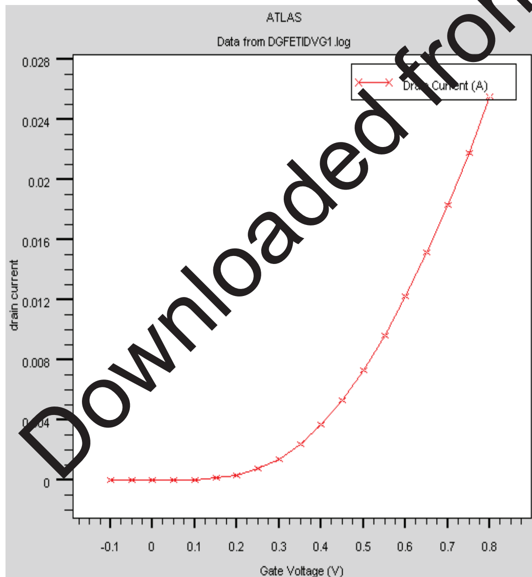

Figure 5 . Simulated transfer characteristic I_{DS}–V_{GS} of the DG n-MOSFET structure.

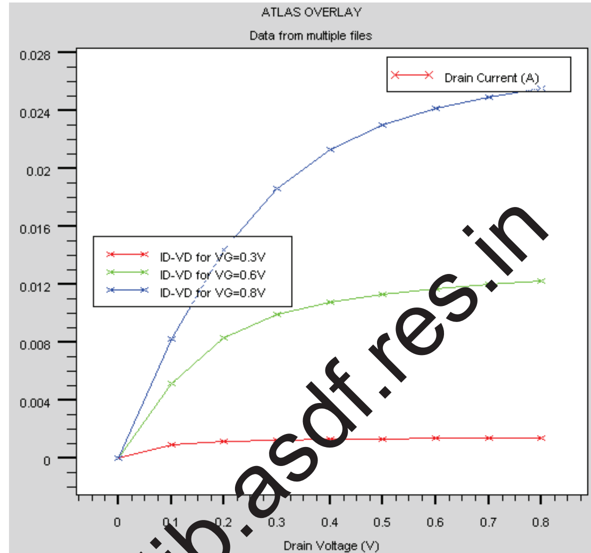

Figure 6. Simulated output characteristic I_{DS}–V_{DS} of the DG n-MOSFET structure.

In order to study the influence of some structure parameters on its electrical characteristics, some parameters are modified. We examine then the effect of these modifications on our DG n-MOSFET drain current.

A. Influence of channel doping variation on I_D current.

Fig 7 shows the output characteristics for different channel doping concentrations.

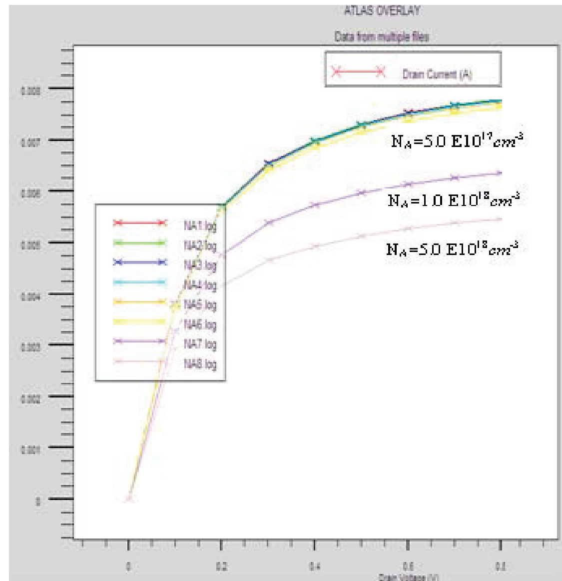

Figure7. DG n-MOSFET output characteristics for different channel doping.

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We can observe that channel doping variation leads to drain current decreasing when doping densities are greater than 5E17/ cm^3. In fact threshold voltage is strongly predisposed by doping variations. Channel doping can be chosen carefully in order to adjust the required threshold voltage.

A. *Influence of channel length L_{ch} variation on I_D current*

Figs. 9, 10 and 11 show the characteristics of the simulated device for different channel lengths L_{ch}.

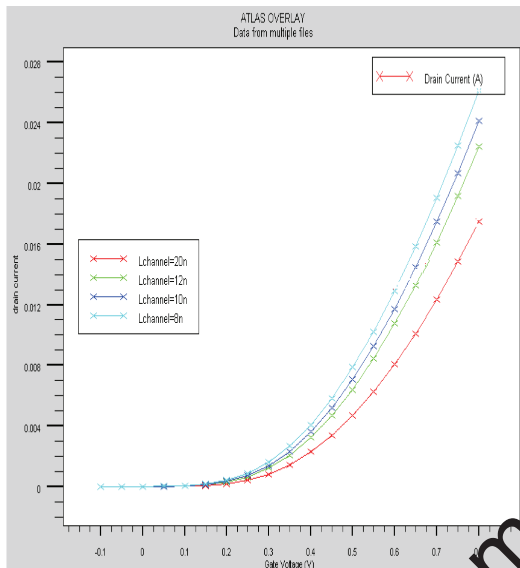

Figure 8. Ids-Vgs characteristics with different L_{ch} with fixed tsi.

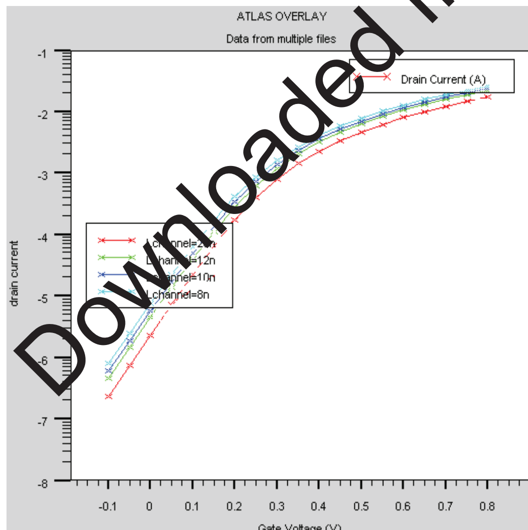

Figure 9. log Ids-Vgs characteristics with different L_{ch} with fixed tsi.

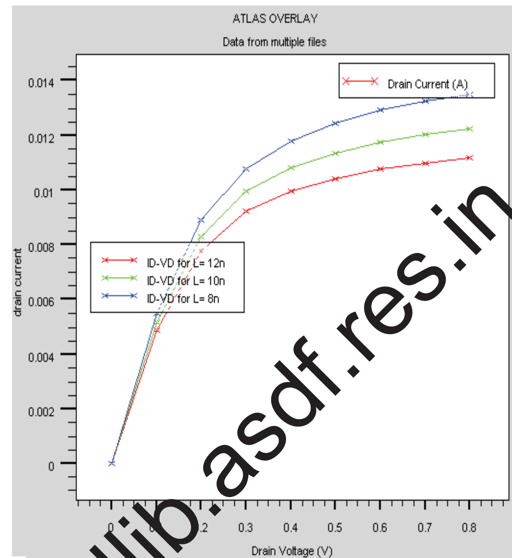

Figure 10. Ids-Vds characteristics with different L_{ch} with fixed tsi.

Threshold voltage is higher for a length of 20 nm compared to a length of 8 nm. Thus we see that V_{th} actually depends on L_{ch} and increases when the length increases. Fig 10 allows observing that the reduction of the channel length results on drain current increasing. If we consider the on-state current device which is considered as an important parameter allowing evaluating the devices operation, we can observe that short channel devices do slightly enhance the on-state current.

B. *Influence of gate length L_G variation on I_D current*

In order to study the gate length variation effect on I_D current the channel length transistor was held constant and equal to 24 nm; however in order to achieve this study, the gate length covers part or the entire channel.

Figs 11 and 12 illustrate the output and the transfer characteristics at different gate lengths.

Saturation drains current decreases strongly with gate length increasing. Threshold voltage roll off can be revealed at shorter gate lengths. Gate length reduction may lead to a bad DIBL characteristic.

From the opinion of fabrication engineering, this will be an important concern for scaling down MOS devices. Without considering the poor SCEs for short L_{ch} devices, it could be concluded that L_G does not drastically modulate the on-state current of DG devices which will be limited because of the relatively high parasitic resistance resulting on the limitation of the on-state current devices.

We can conclude that gate length L_G must be prudently chosen in view of the fact that the gate loss its control on the channel when L_G is very short. Therefore it is important not to reduce the gate length randomly.

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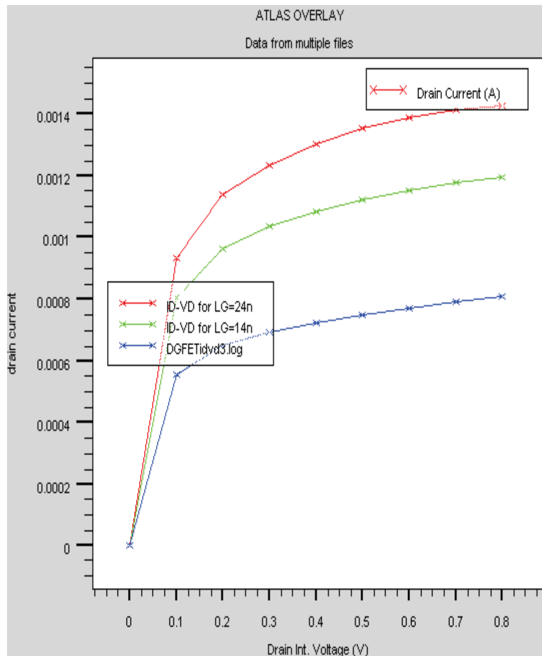

Figure 11. Output characteristics with different L_G values.

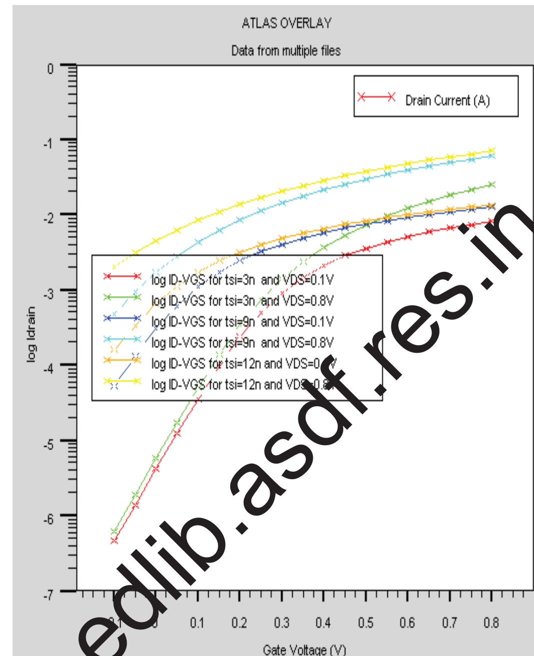

Figure 13. Description of DIBL for Different silicon film thickness t_{si}

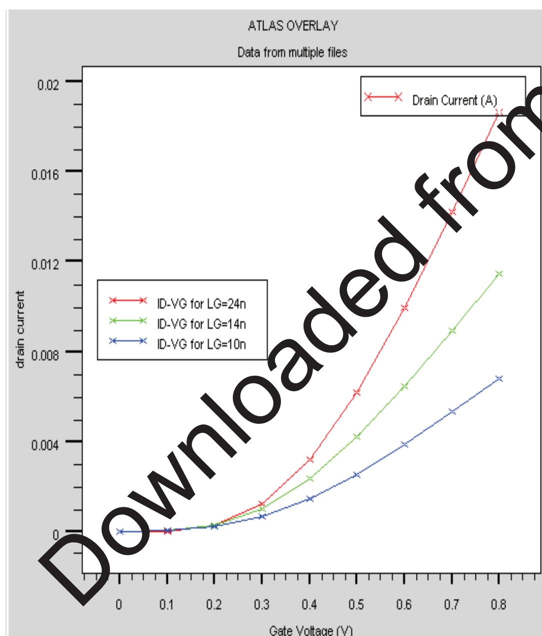

Figure 12. Transfer characteristics with different L_G values.

Fig 13 allows observing that transfer curves with t_{si}=3 nm slightly shows DIBL effects, whereas these curves with t_{si}= 12nm present significant DIBL effects. .

By placing a second gate on the opposite side of the device allowing conceiving a double gate transistor, the gate capacitance of the channel is doubled, and the potential of the channel is better controlled by the gate electrode, thus limiting the off state current.

Furthermore, our simulation results allow observing that the off-state current I_{off} is higher with thicker t_{si} than the off-state current I_{off} with thinner tsi [10]. I_{off} current of our n-DGFET device with the thicker silicon film t_{si} is appreciably elevated compared with the thinner one. Our simulation results allowed observing that reducing the body thickness further decreases the off state current. At the end we can conclude that, devices with a thicker t_{si} owing poor gate controllability have a lesser channel barrier height, present a higher leakage current level, and get a bad result for DIBL effects.

CONCLUSION

The scaling down of conventional MOSFETs according to the International Technology Roadmap for Semiconductors ITRS requires new structures such as DGMOSFETs. These structures allow for higher current drive capability and a better control of short channel effects reducing considerably these SCE that appears under 50nm node. In order to conceive these types of structures numerical devices simulations are required. Variations of

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different structure parameters have been carried out to calculate their influence on the device characteristics. In this work Variations of different DGFET structure parameters have been carried out to calculate the influence of these variations on the device characteristics. At the end of this paper, we observe that simulation results we obtained are comparable to the results encountered in theory and are thus considered very promising.

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